

# CEH2637A

-20V ▲ 65mΩ ▲ -3.3A ▲ Dual Si MOSFET

**SILICON Si MOSFET** ▲ SMD type

Dual P-channel enhancement mode

UL94V-0 rated flame retardant epoxy

TSOP6 package ▲ MSL 3

High dense cell density for extremely low  $R_{DS(ON)}$

**Rugged and reliable**

## MAXIMUM RATINGS

Parameter ( $T_A = 25^{\circ}\text{C}$ , unless otherwise noted)		Characteristics
Drain-Source Voltage	$V_{DS}$	-20V
Gate-Source Voltage	$V_{GS}$	$\pm 12\text{V}$
Continuous Drain Current	$I_D$	-3.3A
Pulsed Drain Current <sup>Note 1</sup>	$I_{DM}$	-13.2A
Maximum Power Dissipation	$P_D$	1.14W
Operating and Storage Temperature Range	$T_J, T_{STG}$	$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$

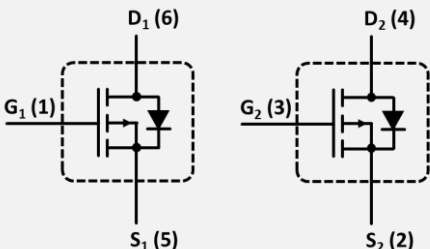
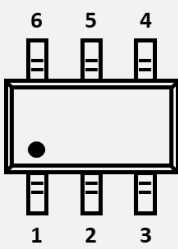
## THERMAL CHARACTERISTICS

Parameter	Symbol	Limit
Thermal Resistance, Junction-to-Ambient <sup>Note 2</sup>	$R_{TH\_JA}$	$110^{\circ}\text{C/W}$

## APPLICATIONS

Data Server Control	DC/DC Converter	Network Devices	Portable Products	USB Storage
				

## PIN DESCRIPTION

Circuit Diagram	Outline - Bottom View	Pin No.	Description
		1 2 3 4 5 6	Gate MOSFET 1 Source MOSFET 2 Gate MOSFET 2 Drain MOSFET 2 Source MOSFET 1 Drain MOSFET 1

## ELECTRICAL CHARACTERISTICS ▲ $T_A = 25^\circ\text{C}$ , unless otherwise noted

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	$BV_{DSS}$	-20			V
Zero Gate Voltage Drain Current	$V_{DS} = -20V, V_{GS} = 0V$	$I_{DSS}$			-1	$\mu A$
Gate Body Leakage Current, Forward	$V_{GS} = 12V, V_{DS} = 0V$	$I_{GSSF}$			100	nA
Gate Body Leakage Current, Reverse	$V_{GS} = -12V, V_{DS} = 0V$	$I_{GSSR}$			-100	nA
<b>On Characteristics</b> <sup>Note 3</sup>						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	$V_{GS(th)}$	-0.4		-1	V
Static Drain-Source On-Resistance	$V_{GS} = -4.5V, I_D = -3A$	$R_{DS(ON)}$		60	65	m $\Omega$
Static Drain-Source On-Resistance	$V_{GS} = -2.5V, I_D = -2A$	$R_{DS(ON)}$		80	100	m $\Omega$
Static Drain-Source On-Resistance	$V_{GS} = -1.8V, I_D = -1A$	$R_{DS(ON)}$		110	150	m $\Omega$
<b>Dynamic Characteristics</b> <sup>Note 4</sup>						
Input Capacitance	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$	$C_{ISS}$		405		pF
Output Capacitance	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$	$C_{OSS}$		70		pF
Reverse Transfer Capacitance	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$	$C_{RSS}$		55		pF
<b>Switching Characteristics</b> <sup>Note 4</sup>						
Turn-On Delay Time	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A, R_{G(ext)} = 6\Omega$	$t_{D(ON)}$		15		ns
Turn-On Rise Time	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A, R_{G(ext)} = 6\Omega$	$t_R$		8		ns
Turn-Off Delay Time	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A, R_{G(ext)} = 6\Omega$	$t_{D(OFF)}$		47		ns
Turn-Off Fall Time	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A, R_{G(ext)} = 6\Omega$	$t_F$		15		ns
Total Gate Charge	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A$	$Q_G$		5.7		nC
Gate Source Charge	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A$	$Q_{GS}$		0.5		nC
Gate Drain Charge	$V_{DD} = -15V, V_{GS} = -4.5V, I_D = -3A$	$Q_{GD}$		1.8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>Note 2</sup>		$I_S$			-0.95	A
Drain-Source Diode Forward Voltage <sup>Note 3</sup>	$V_{GS} = 0V, I_S = -8A$	$V_{SD}$			-1.2	V

### Notes

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: Surface Mounted on FR4 Board,  $t \leq 5$  sec.
- 3: Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
- 4: Guaranteed by design, not subject to production testing.

## REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 1 • Output Characteristics

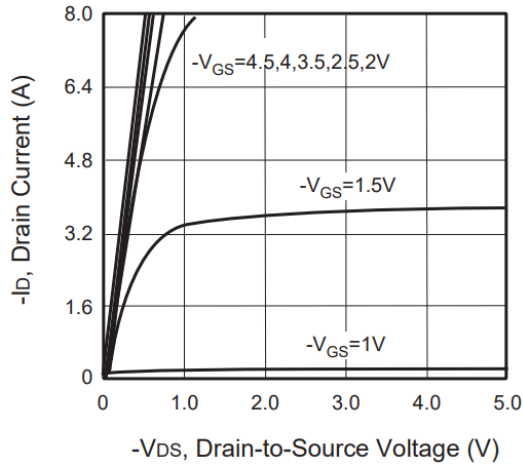


Fig. 2 • Transfer Characteristics

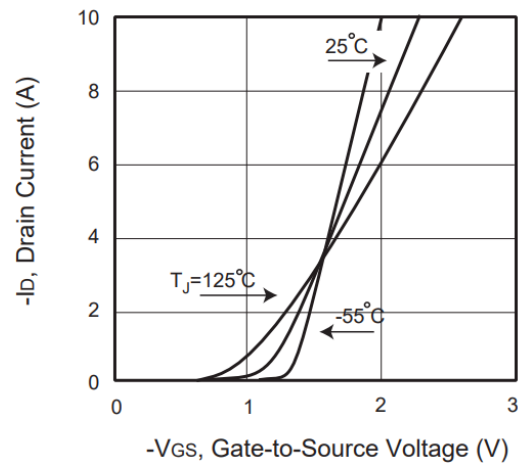


Fig. 3 • Capacitance

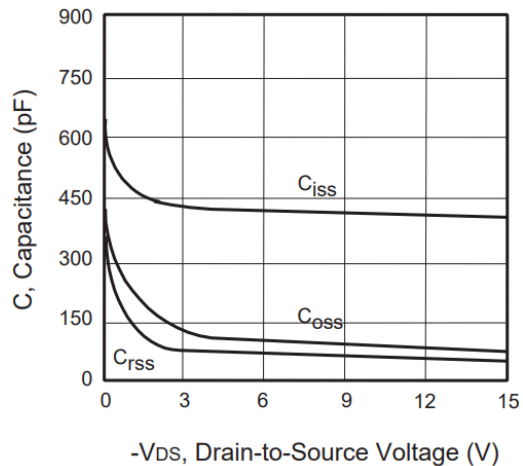


Fig. 4 • On-Resistance Variation with Temperature

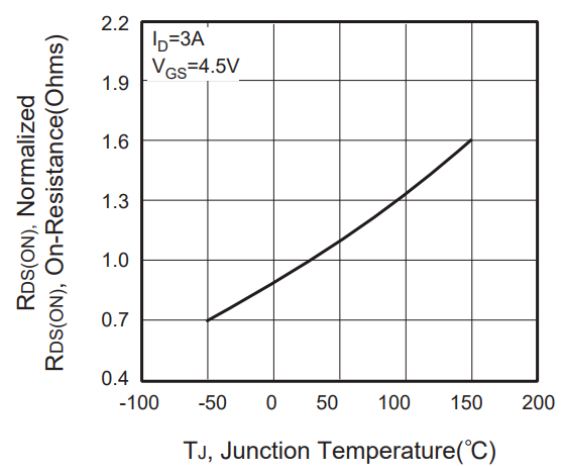


Fig. 5 • Gate Threshold Variation with Temperature

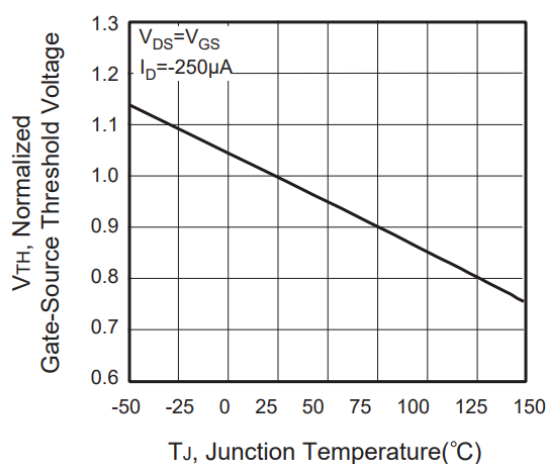
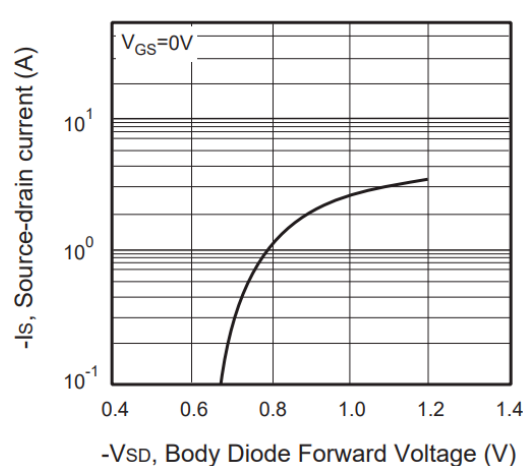


Fig. 6 • Body Diode Forward Voltage Variation with Source Current



## REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 7 • Gate Charge

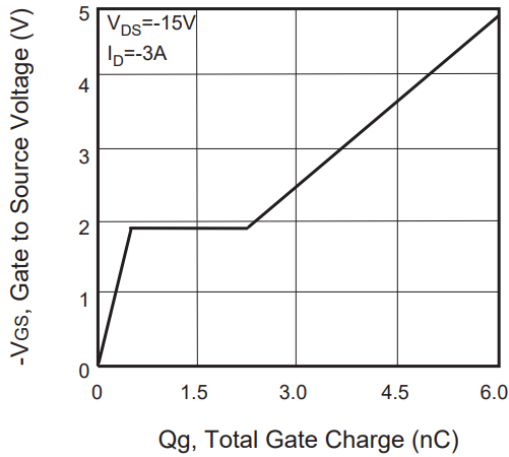


Fig. 8 • Maximum Safe Operating Area

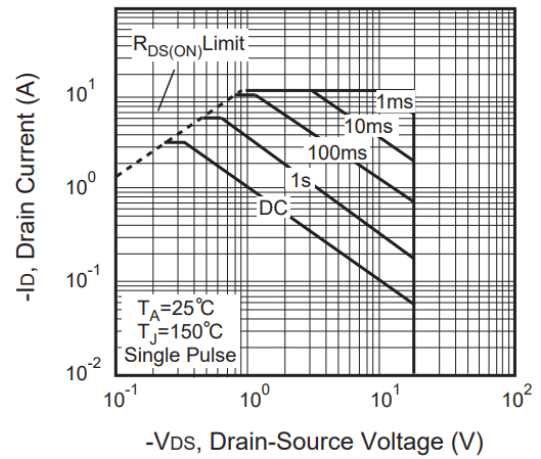


Fig. 9 • Breakdown Voltage Variation vs. Temperature

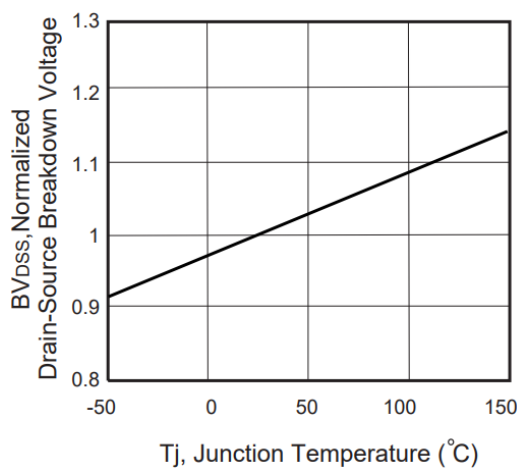


Fig. 10 • Switching Test Circuit

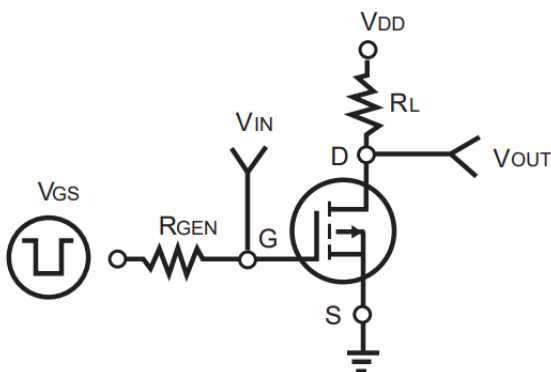
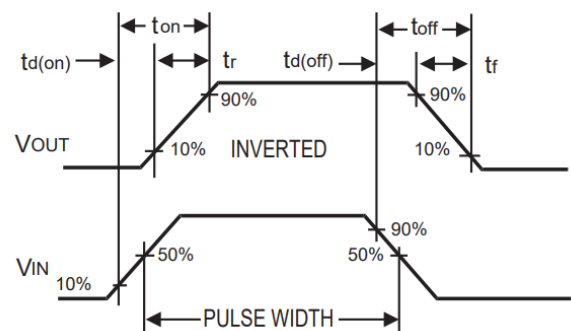
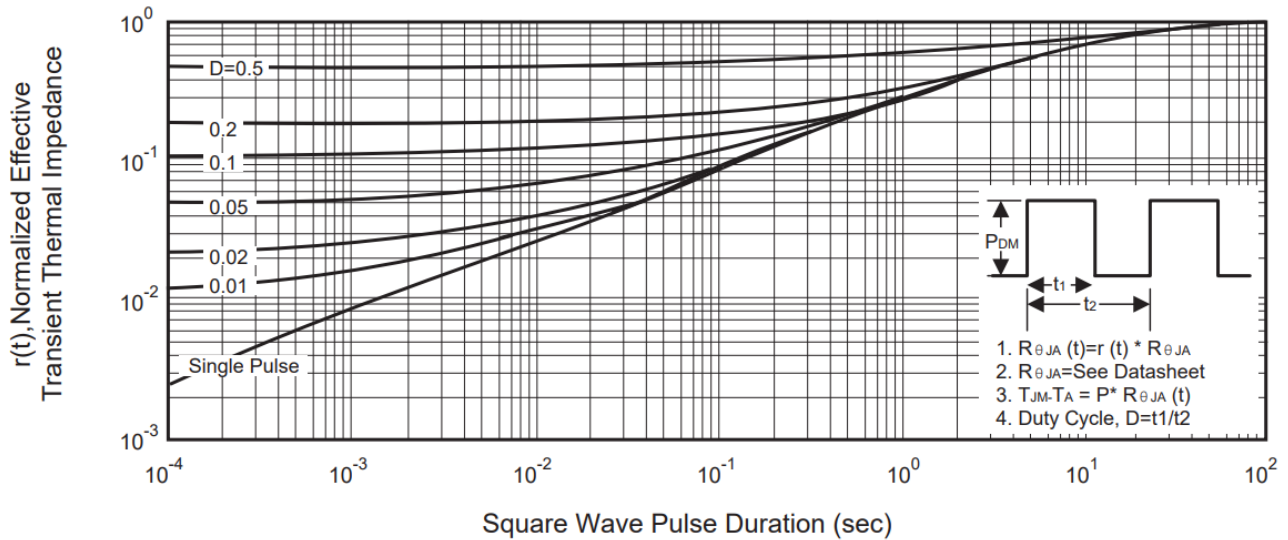


Fig. 11 • Switching Waveforms

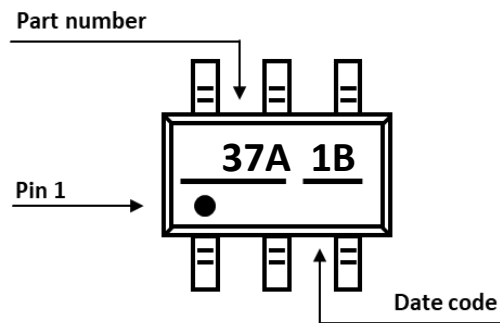


## REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 12 • Normalized Thermal Transient Impedance Curve

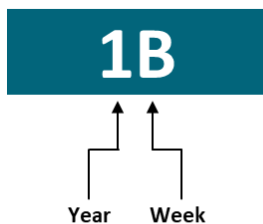


## PART MARKING



## DATE CODE

Example: 1B



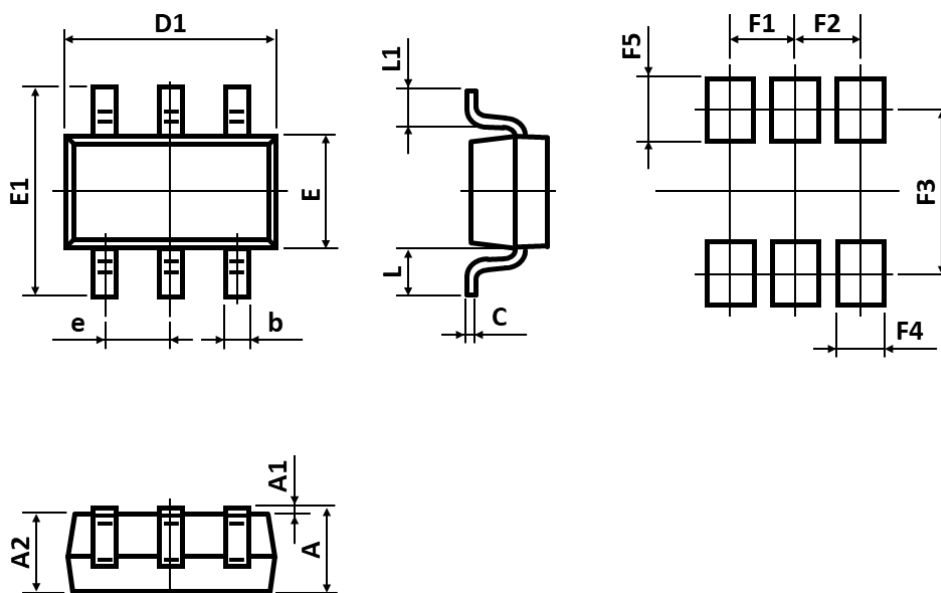
Coding list for „Week“

A	B	C	D	E	F	G	H	I
1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18
J	K	L	M	N	O	P	Q	R
19-20	21-22	23-24	25-26	27-28	29-30	31-32	33-34	35-36
S	T	U	V	W	X	Y	Z	
37-38	39-40	41-42	43-44	45-46	47-48	49-50	51-52	

Coding list for „Year“

0	1	2	3	4
2020	2021	2022	2023	2024
5	6	7	8	9
2025	2026	2027	2028	2029

## PACKAGE OUTLINE AND RECOMMENDED PAD LAYOUT



Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
A	0.800	-	1.250
A1	0.000	-	0.130
A2	0.700	-	1.200
b	0.300	-	0.500
C	0.090	-	0.200
D1	2.800	-	3.100

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F1	-	0.950	-
F2	-	0.950	-
F3	-	2.600	-

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
E	1.500	-	1.700
E1	2.500	-	3.100
e	0.950 (TYP)		
L	0.350	-	0.800
L1	0.300	-	0.550

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F4	-	0.700	-
F5	-	1.000	-

Notes: 1. The suggested land pattern dimensions have been provided for reference only.  
2. For further information, please reference document IPC-7351A.

## ORDERING INFORMATION

Part Number	Package	Packing	Reel Qty.	Inner Box Qty.
CEH2637A	TSOP 6	Reel	3,000pcs	15,000pcs

## REEL DIMENSIONS ▲ All dimensions in mm



Tape Size	Reel Size	M	N	T	H	K	S
8mm	Ø180	Ø178.00 ±1.00	Ø54.00 ±0.50	1.20 ±0.20	20.00 ±1.00	13.30 ±0.30	3.00 ±1.00

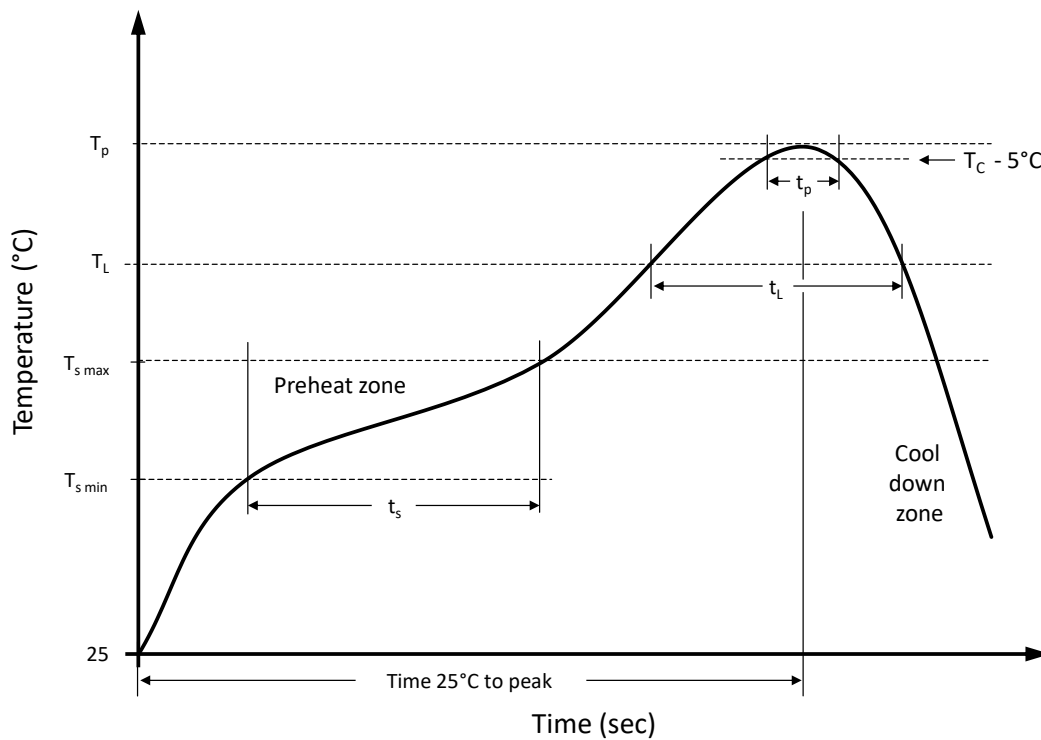
## TAPE DIMENSIONS ▲ All dimensions in mm



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSOP6	3.20 ±0.10	3.20 ±0.10	1.35 ±0.10	1.00 ±0.10	1.50 ±0.10	8.00 ±0.10	1.75 ±0.10	3.50 ±0.10	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.20 ±0.02

Note: All dimensions meet EIA-481-D requirements.

## RECOMMENDED REFLOW SOLDERING PROFILE



### Recommended reflow soldering conditions ▲ Refer to JEDEC J-STD-020E

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	$T_{s \min}$	100 °C	150 °C
Preheat temperature max.	$T_{s \max}$	150 °C	200 °C
Preheat time $t_s$ from $T_{s \min}$ to $T_{s \max}$	$t_s$	120 seconds	120 seconds
Ramp-up rate ( $T_L$ to $T_p$ )		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	$T_L$	183 °C	217 °C
Time $t_L$ maintained above $T_L$	$t_L$	150 seconds max.	150 seconds max.
Peak package body temperature	$T_p$	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	$t_p$	20 seconds max.	30 seconds max.
Ramp-down rate ( $T_L$ to $T_p$ )		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes



## REVISION TABLE

Revision	Date	Status	Notes
001	30/09/2022	Initial release	Initial publication

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