



# CEU1010L

100V ▲ 8.5mΩ ▲ 63A ▲ Si MOSFET

SILICON Si MOSFET ▲ SMD type

N-channel enhancement mode

UL94V-0 rated flame retardant epoxy

TO252 (DPAK) package ▲ MSL 3

Super high dense cell density for extremely low  $R_{DS(ON)}$

**High power and current handling capability**

## MAXIMUM RATINGS

Parameter ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)		Characteristics
Drain-Source Voltage	$V_{DS}$	100V
Gate-Source Voltage	$V_{GS}$	$\pm 20\text{V}$
Continuous Drain Current at $T_C = 25^\circ\text{C}$	$I_D$	63A
Continuous Drain Current at $T_C = 100^\circ\text{C}$	$I_D$	40A
Pulsed Drain Current <sup>Note 1</sup>	$I_{DM}$ <sup>Note 4</sup>	252A
Maximum Power Dissipation at $T_C = 25^\circ\text{C}$	$P_D$	69W
Power Dissipation Derating above $25^\circ\text{C}$	$\Delta P_D$	$0.55\text{W}/^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>Note 5</sup>	$E_{AS}$	74mJ
Single Pulsed Avalanche Current <sup>Note 5</sup>	$I_{AS}$	38.5A
Operating and Storage Temperature Range	$T_J, T_{STG}$	$-55^\circ\text{C}$ to $+150^\circ\text{C}$

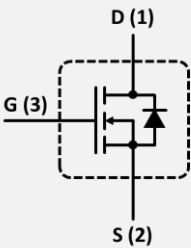
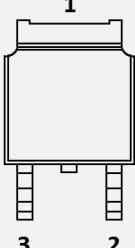
## THERMAL CHARACTERISTICS

Parameter	Symbol	Limit
Thermal Resistance, Junction-to-Case	$R_{TH\_JC}$	$1.8^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient <sup>Note 2</sup>	$R_{TH\_JA}$	$50^\circ\text{C}/\text{W}$

## APPLICATIONS

Battery Management Systems	E-Bike	Industrial Control	Power Inverter	UPS
				

## PIN DESCRIPTION

Circuit Diagram	Outline - Bottom View	Pin No.	Description
		1 2 3	Drain Source Gate

## ELECTRICAL CHARACTERISTICS ▲ $T_C = 25^\circ\text{C}$ , unless otherwise noted

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	100			V
Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$	$I_{DSS}$			1	$\mu A$
Gate Body Leakage Current, Forward	$V_{GS} = 20V, V_{DS} = 0V$	$I_{GSSF}$			100	nA
Gate Body Leakage Current, Reverse	$V_{GS} = -20V, V_{DS} = 0V$	$I_{GSSR}$			-100	nA
<b>On Characteristics</b> <sup>Note 3</sup>						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(th)}$	1		2.5	V
Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 20A$	$R_{DS(ON)}$		8.5	9.8	m $\Omega$
Static Drain-Source On-Resistance	$V_{GS} = 4.5V, I_D = 20A$	$R_{DS(ON)}$		11.4	13	m $\Omega$
<b>Dynamic Characteristics</b> <sup>Note 3</sup>						
Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	$C_{ISS}$		1430		pF
Output Capacitance	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	$C_{OSS}$		290		pF
Reverse Transfer Capacitance	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	$C_{RSS}$		5		pF
<b>Switching Characteristics</b> <sup>Note 3</sup>						
Turn-On Delay Time	$V_{DD} = 50V, V_{GS} = 10V, I_D = 20A, R_{G(ext)} = 10\Omega$	$t_{D(ON)}$		15		ns
Turn-On Rise Time	$V_{DD} = 50V, V_{GS} = 10V, I_D = 20A, R_{G(ext)} = 10\Omega$	$t_R$		7		ns
Turn-Off Delay Time	$V_{DD} = 50V, V_{GS} = 10V, I_D = 20A, R_{G(ext)} = 10\Omega$	$t_{D(OFF)}$		43		ns
Turn-Off Fall Time	$V_{DD} = 50V, V_{GS} = 10V, I_D = 20A, R_{G(ext)} = 10\Omega$	$t_F$		16		ns
Total Gate Charge	$V_{DD} = 50V, V_{GS} = 4.5V, I_D = 20A$	$Q_G$		14		nC
Gate Source Charge	$V_{DD} = 50V, V_{GS} = 4.5V, I_D = 20A$	$Q_{GS}$		3		nC
Gate Drain Charge	$V_{DD} = 50V, V_{GS} = 4.5V, I_D = 20A$	$Q_{GD}$		8		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>Note 2</sup>		$I_S$			57	A
Drain-Source Diode Forward Voltage <sup>Note 2</sup>	$V_{GS} = 0V, I_S = 20A$	$V_{SD}$			1.2	V

### Notes

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
- 3: Guaranteed by design, not subject to production testing.
- 4: Pulse width limited by safe operating area.
- 5:  $L = 0.1mH, I_{AS} = 38.5A, V_{DD} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$

## REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 1 • Output Characteristics

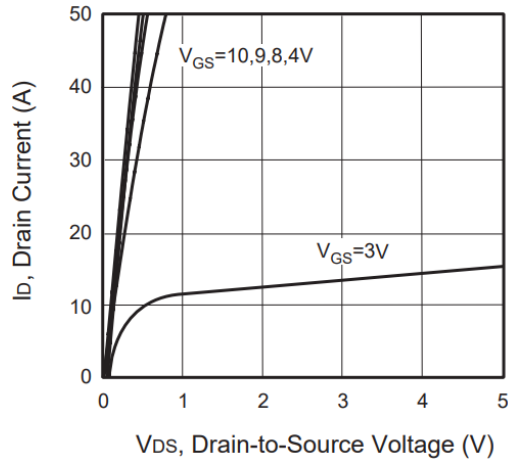


Fig. 2 • Transfer Characteristics

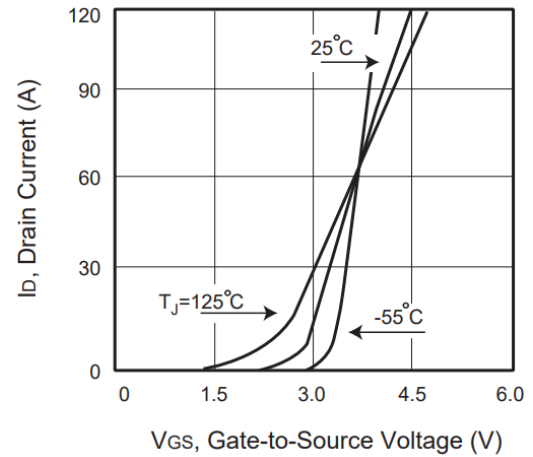


Fig. 3 • Capacitance

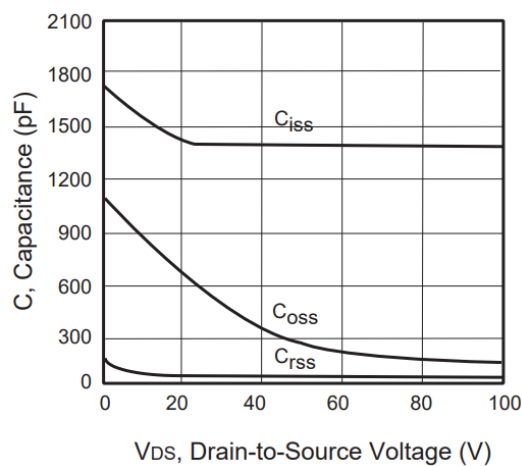


Fig. 4 • On-Resistance Variation with Temperature

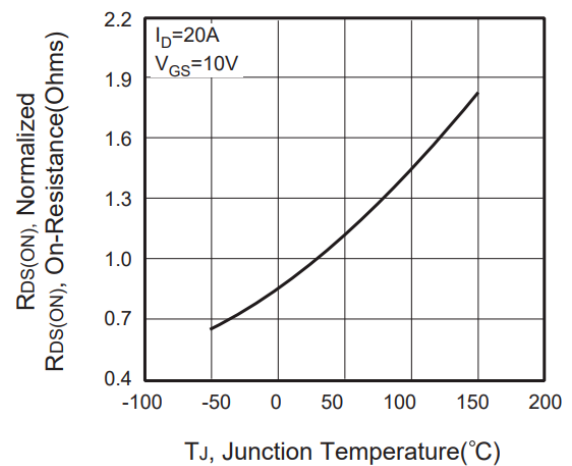


Fig. 5 • Gate Threshold Variation with Temperature

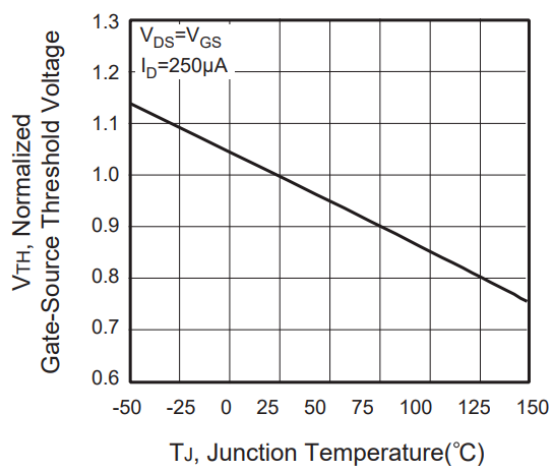
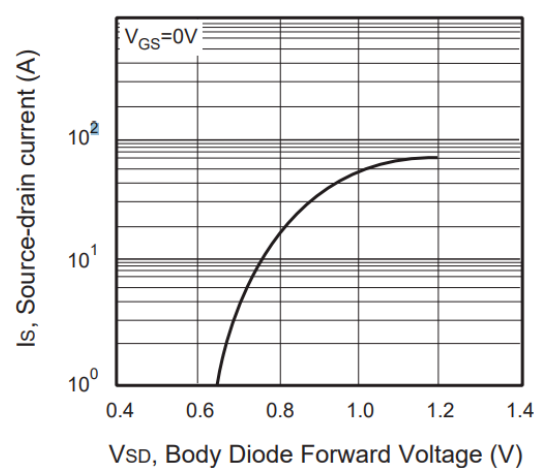


Fig. 6 • Body Diode Forward Voltage Variation with Source Current



## REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 7 • Gate Charge

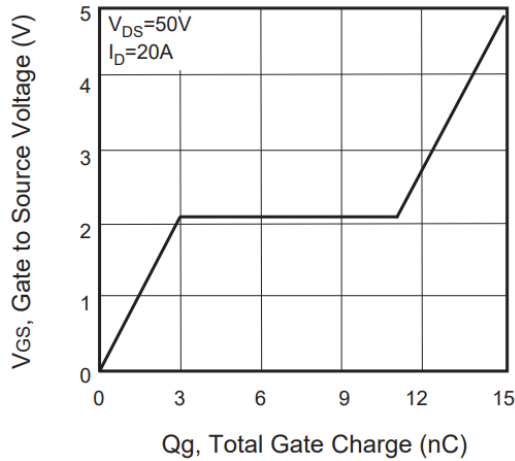


Fig. 8 • Maximum Safe Operating Area

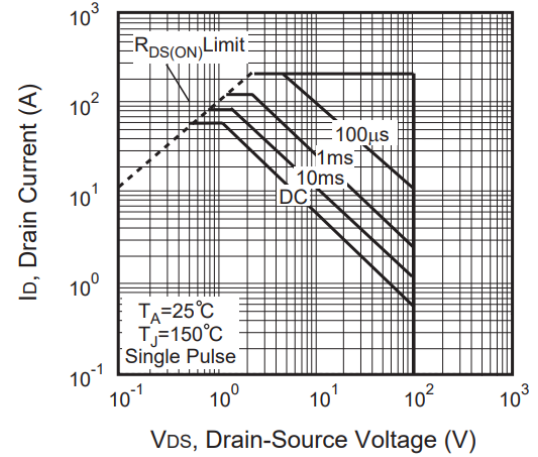


Fig. 9 • Breakdown Voltage Variation vs. Temperature

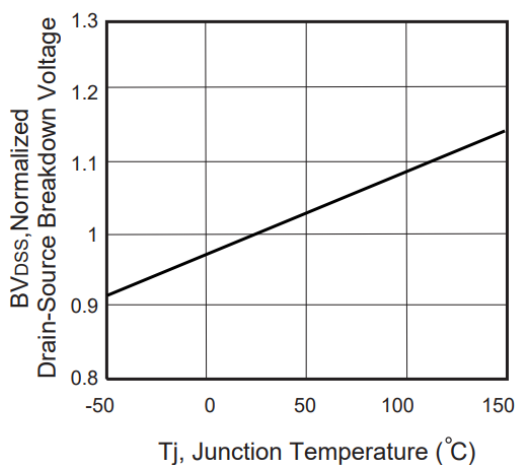


Fig. 10 • Switching Test Circuit

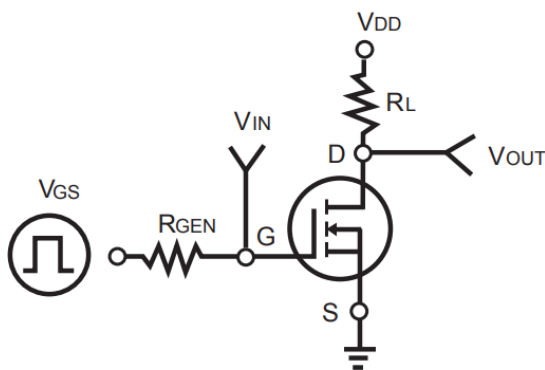
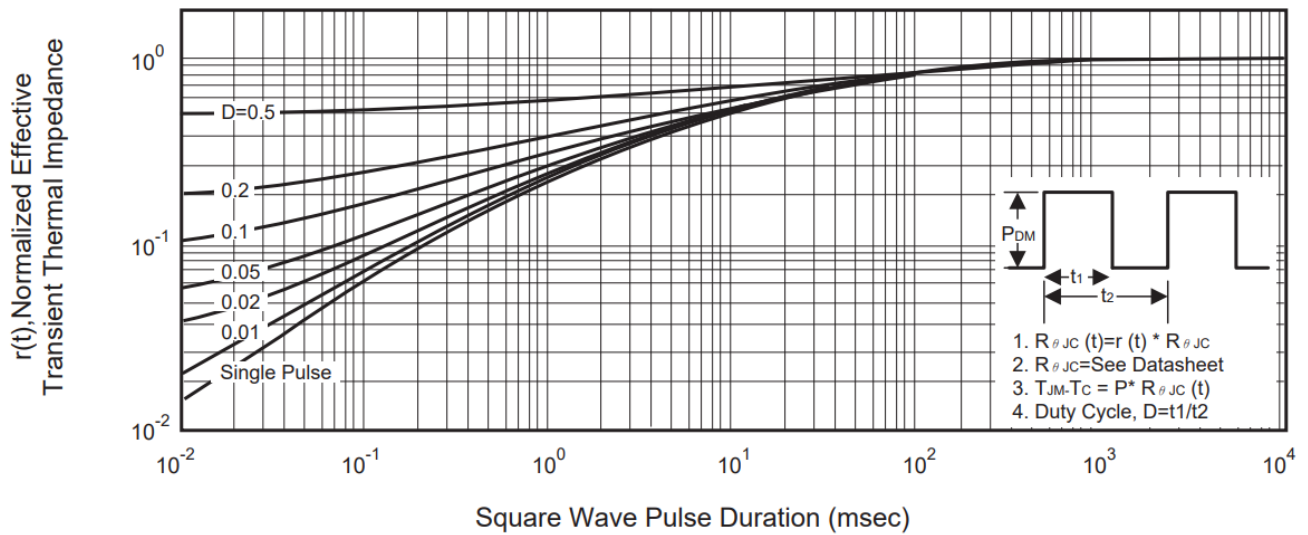


Fig. 11 • Switching Waveforms

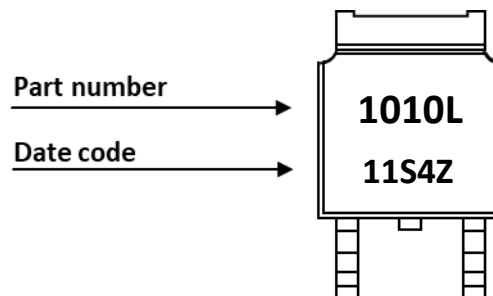


## REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 12 • Normalized Thermal Transient Impedance Curve



## PART MARKING



## DATE CODE

Example: 11S4Z



Coding list for „Day“

1	2	3	4	5	6	7	8	9	A
01	02	03	04	05	06	07	08	09	10
B	C	D	E	F	G	H	I	J	K
11	12	13	14	15	16	17	18	19	20
L	M	N	O	P	Q	R	S	T	U
21	22	23	24	25	26	27	28	29	30
V									
31									

Coding list for „Month“

1	2	3	4	5	6
Jan	Feb	Mar	Apr	May	Jun
7	8	9	A	B	C
Jul	Aug	Sep	Oct	Nov	Dec

Coding list for „Year“

0	1	2	3	4
2020	2021	2022	2023	2024
5	6	7	8	9
2025	2026	2027	2028	2029

## PACKAGE OUTLINE



Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
A	2.20	2.30	2.38
A1	0.00	-	0.20
A2	0.90	1.07	1.17
b	0.68	0.78	0.90
b3	5.23	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30 REF		
E	6.40	6.60	6.73
E1	4.63	-	-

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
e		2.286 BSC	
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90 REF		
L2	0.51 BSC		
L3	0.88	-	1.28
L4	0.50	.	1.00
L5	1.65	1.80	1.95
θ	0°	-	8°

## ORDERING INFORMATION

Part Number	Package	Packing	Reel Qty.	Inner Box Qty.	Outer Box Qty.
CEU1010L	TO252 (DPAK)	Reel	2,500pcs	5,000pcs	40,000pcs

## RECOMMENDED PAD LAYOUT



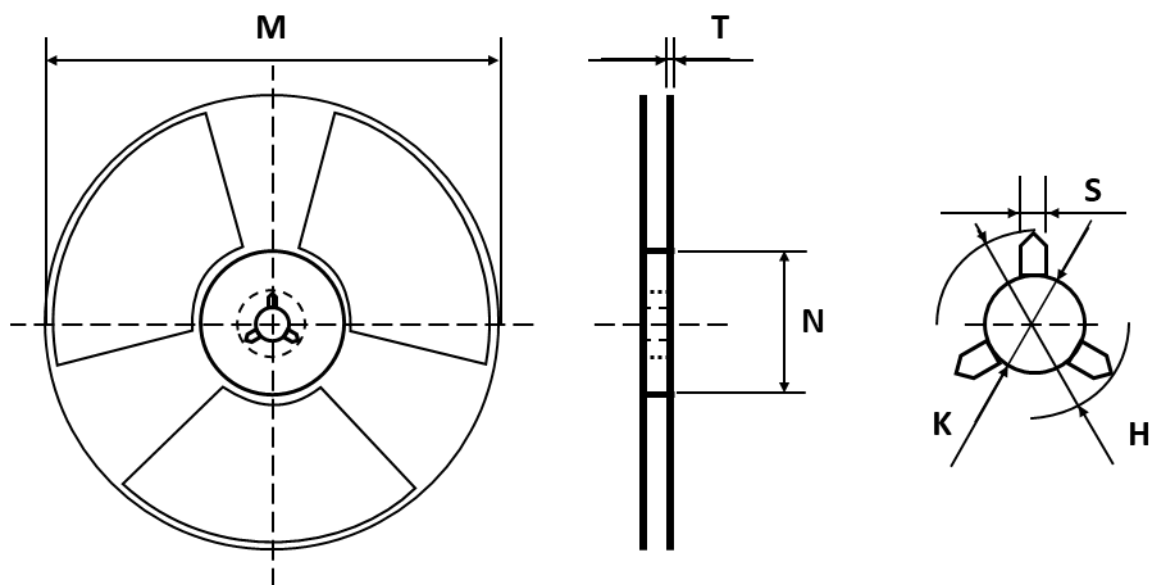
Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F1	-	6.00	-
F2	-	6.25	-
F3	-	1.40	-
F4	-	2.29	-

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F5	-	2.29	-
F6	-	1.40	-
F7	-	3.00	-
F8	-	6.50	-

### Notes:

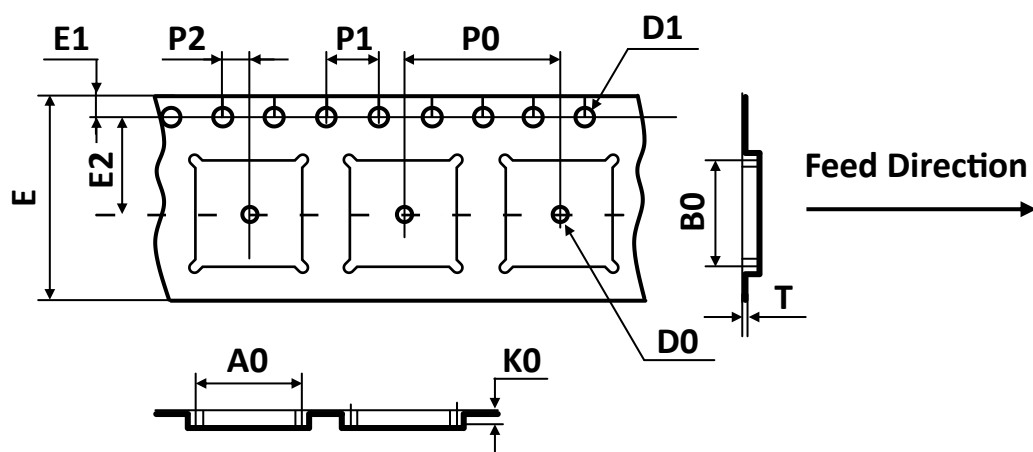
1. The suggested land pattern dimensions have been provided for reference only.
2. For further information, please reference document IPC-7351A.

## REEL DIMENSIONS ▲ All dimensions in mm



Tape Size	Reel Size	M	N	T	H	K	S
16mm	Ø330	Ø330.00	Ø100.00	2.10	22.00	13.00	2.00
		±2.00	±0.50	±0.20	±0.50	+0.50 -0.20	+0.50 -0.20

## TAPE DIMENSIONS ▲ All dimensions in mm

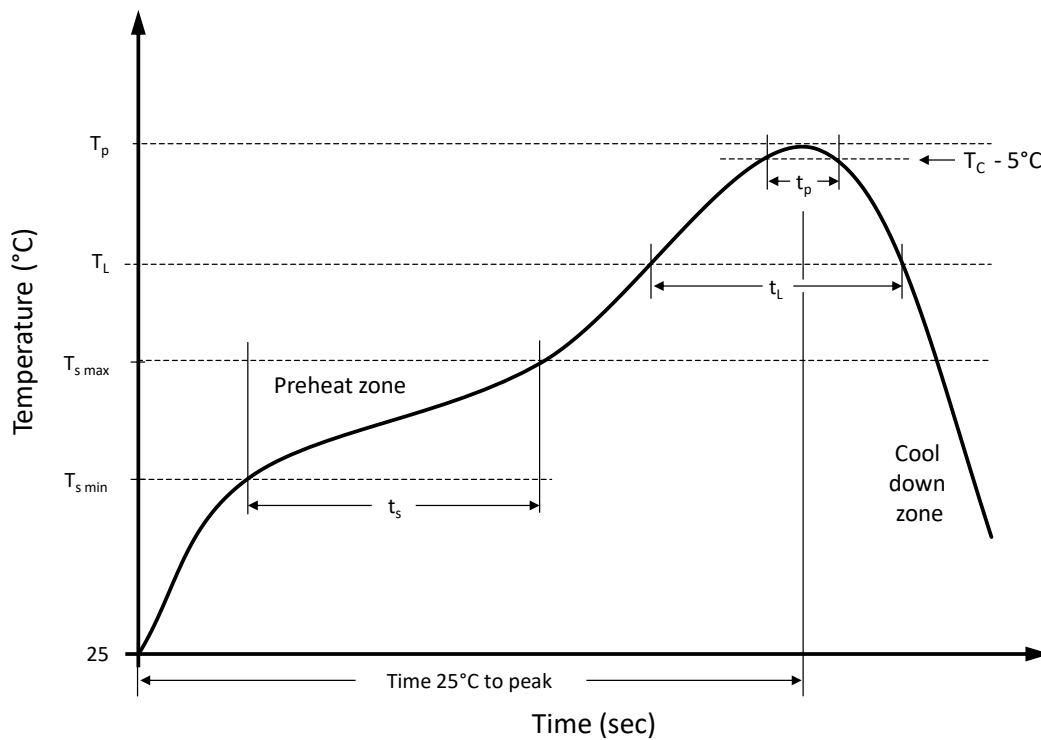


Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO252 (DPAK)	6.90	10.50	2.70	1.50	1.50	16.00	1.75	7.50	8.00	4.00	2.00	0.30
	±0.10	±0.10	±0.10	MIN	±0.10	+0.30 -0.20	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05

**Note:** All dimensions meet EIA-481-D requirements.



## RECOMMENDED REFLOW SOLDERING PROFILE



### Recommended reflow soldering conditions ▲ Refer to JEDEC J-STD-020E

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	T <sub>s min</sub>	100 °C	150 °C
Preheat temperature max.	T <sub>s max</sub>	150 °C	200 °C
Preheat time t <sub>s</sub> from T <sub>s min</sub> to T <sub>s max</sub>	t <sub>s</sub>	120 seconds	120 seconds
Ramp-up rate (T <sub>L</sub> to T <sub>p</sub> )		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	T <sub>L</sub>	183 °C	217 °C
Time t <sub>L</sub> maintained above T <sub>L</sub>	t <sub>L</sub>	150 seconds max.	150 seconds max.
Peak package body temperature	T <sub>p</sub>	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	t <sub>p</sub>	20 seconds max.	30 seconds max.
Ramp-down rate (T <sub>L</sub> to T <sub>p</sub> )		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes

## REVISION TABLE

Revision	Date	Status	Notes
001	30/09/2022	Initial release	Initial publication

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