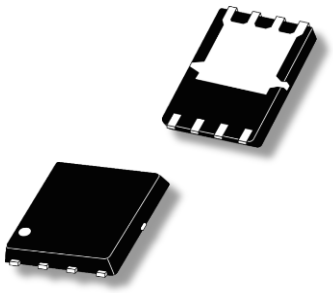

CEZ16R10LA

100V ▲ 13.4mΩ ▲ 31A ▲ Si MOSFET

SILICON Si MOSFET ▲ SMD type
N-channel enhancement mode
UL94V-0 rated flame retardant epoxy
PPAK5x6 package ▲ MSL 3
Super high dense cell density for extremely low $R_{DS(ON)}$
High power and current handling capability

MAXIMUM RATINGS

Parameter (T_A = 25°C, unless otherwise noted)		Characteristics
Drain-Source Voltage	V_{DS}	100V
Gate-Source Voltage	V_{GS}	±20V
Continuous Drain Current at R_{TH_JC}	I_D	31A
Continuous Drain Current at R_{TH_JA}	I_D	14.7A
Pulsed Drain Current at R_{TH_JC} Note 1	I_{DM}	124A
Pulsed Drain Current at R_{TH_JA} Note 1	I_{DM}	58.8A
Maximum Power Dissipation	P_D	27.8W
Single Pulsed Avalanche Energy Note 5	E_{AS}	10mJ
Single Pulsed Avalanche Current Note 5	I_{AS}	4.5A
Operating and Storage Temperature Range	T_J, T_{STG}	-55°C to +150°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Limit
Thermal Resistance, Junction-to-Case	R_{TH_JC}	4.5°C/W
Thermal Resistance, Junction-to-Ambient Note 2	R_{TH_JA}	20°C/W

APPLICATIONS

Battery Management Systems	E-Bike	Industrial Control	Power Inverter	UPS

PIN DESCRIPTION

Circuit Diagram	Outline ▪ Bottom View	Pin No.	Description
D (5), G (4), S (1,2,3)	5, 4 3 2 1	1	Source
		2	Source
		3	Source
		4	Gate
		5	Drain

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ELECTRICAL CHARACTERISTICS ▲ T_A = 25°C, unless otherwise noted

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	100			V
Zero Gate Voltage Drain Current	V_{DS} = 100V, V_{GS} = 0V	I_{DSS}			1	μA
Gate Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0V	I_{GSSF}			100	nA
Gate Body Leakage Current, Reverse	V_{GS} = -20V, V_{DS} = 0V	I_{GSSR}			-100	nA
On Characteristics Note 3						
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(th)}$	1		2.5	V
Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 20A	$R_{DS(ON)}$		13.4	16	mΩ
Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 10A	$R_{DS(ON)}$		18.4	24	mΩ
Dynamic Characteristics Note 4						
Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	C_{ISS}		900		pF
Output Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	C_{OSS}		205		pF
Reverse Transfer Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	C_{RSS}		15		pF
Switching Characteristics Note 4						
Turn-On Delay Time	V_{DD} = 50V, V_{GS} = 10V, I_D = 1A, $R_{G(ext)}$ = 6Ω	$t_{D(ON)}$		17		ns
Turn-On Rise Time	V_{DD} = 50V, V_{GS} = 10V, I_D = 1A, $R_{G(ext)}$ = 6Ω	t_R		4		ns
Turn-Off Delay Time	V_{DD} = 50V, V_{GS} = 10V, I_D = 1A, $R_{G(ext)}$ = 6Ω	$t_{D(OFF)}$		42		ns
Turn-Off Fall Time	V_{DD} = 50V, V_{GS} = 10V, I_D = 1A, $R_{G(ext)}$ = 6Ω	t_F		20		ns
Total Gate Charge	V_{DS} = 50V, V_{GS} = 4.5V, I_D = 20A	Q_G		11.5		nC
Gate Source Charge	V_{DS} = 50V, V_{GS} = 4.5V, I_D = 20A	Q_{GS}		1.7		nC
Gate Drain Charge	V_{DS} = 50V, V_{GS} = 4.5V, I_D = 20A	Q_{GD}		7.8		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current Note3		I_S			23	A
Drain-Source Diode Forward Voltage Note3	V_{GS} = 0V, I_S = 20A	V_{SD}			1.2	V

Notes

1: Repetitive Rating: Pulse width limited by maximum junction temperature

2: Surface Mounted on FR4 Board, t ≤ 10 sec

3: Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4: Guaranteed by design, not subject to production testing.

5: L = 1mH, I_{AS} = 4.5A, V_{DD} = 24V, R_G = 25Ω, Starting T_J = 25°C

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REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 1 ▪ Output Characteristics

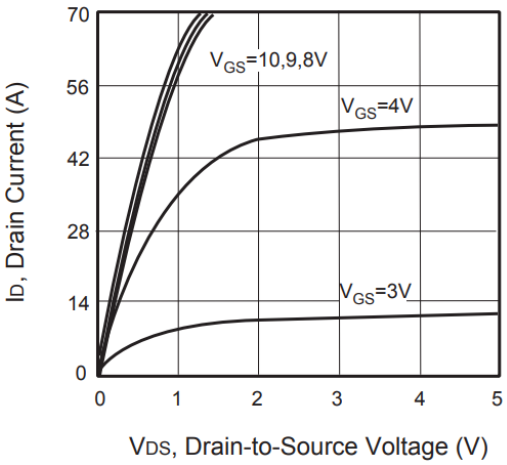


Fig. 2 ▪ Transfer Characteristics

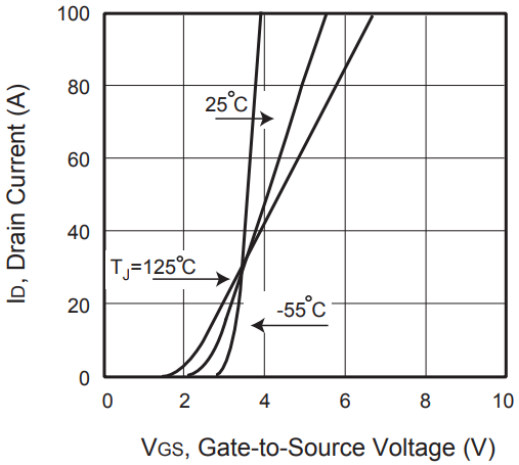


Fig. 3 ▪ Capacitance

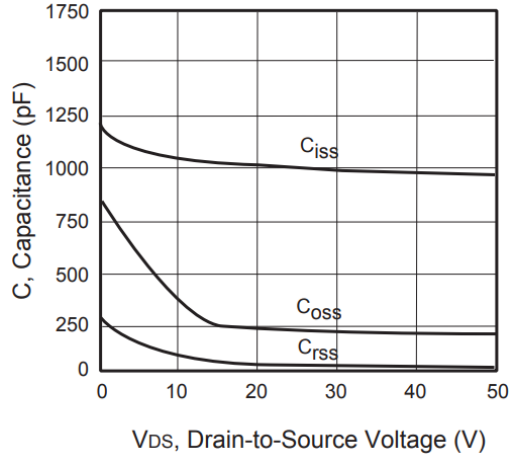


Fig. 4 ▪ On-Resistance Variation with Temperature

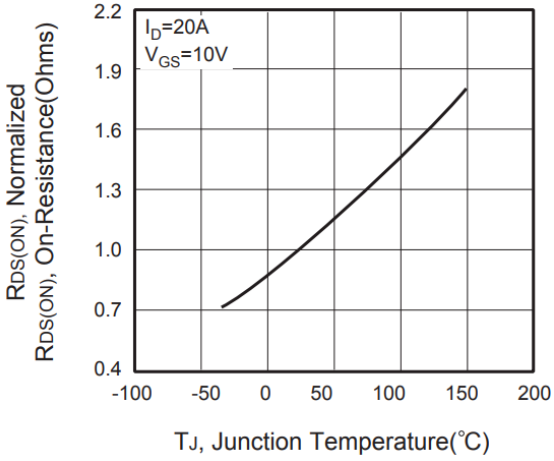


Fig. 5 ▪ Gate Threshold Variation with Temperature

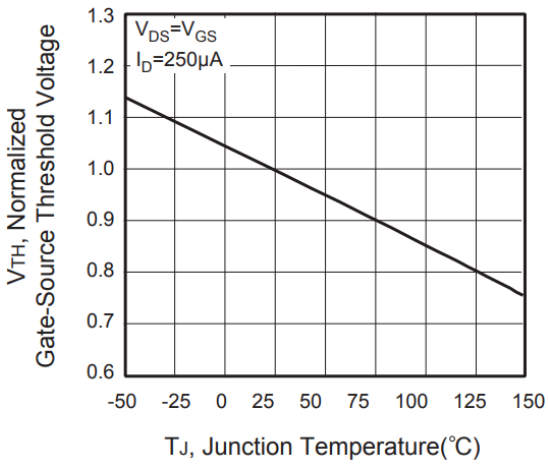
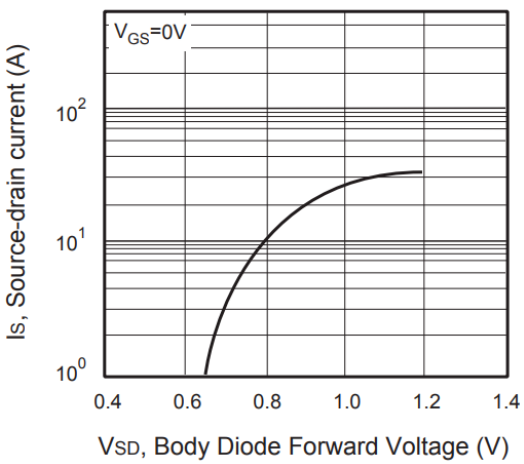


Fig. 6 ▪ Body Diode Forward Voltage Variation with Source Current



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REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 7 ▪ Gate Charge

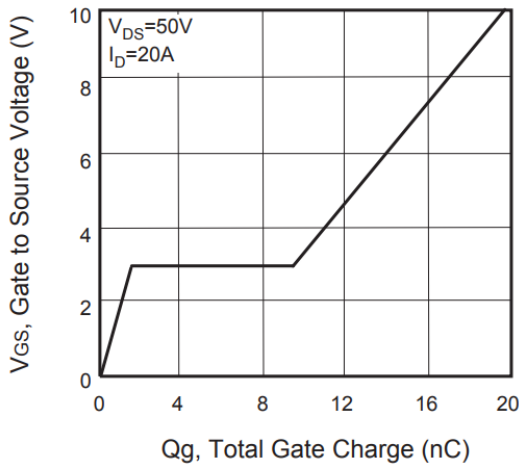


Fig. 8 ▪ Maximum Safe Operating Area

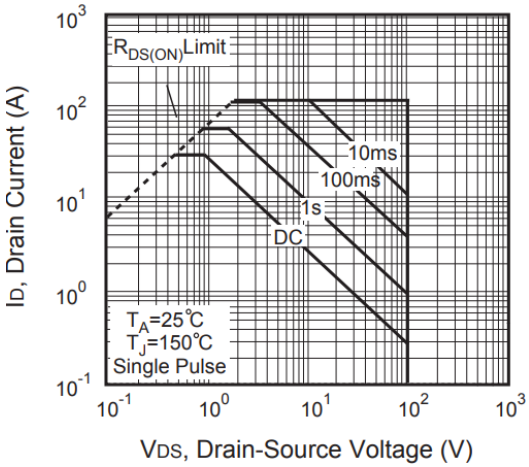


Fig. 9 ▪ Breakdown Voltage Variation vs. Temperature

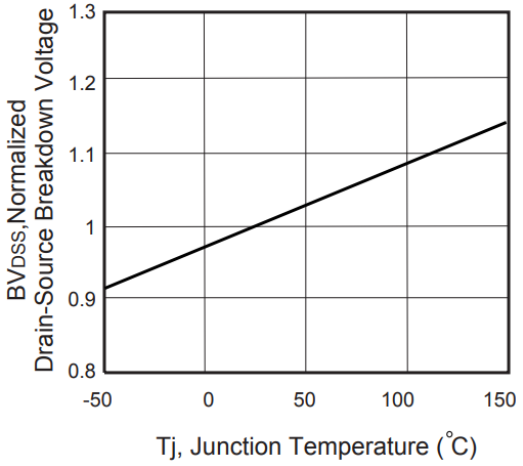


Fig. 10 ▪ Switching Test Circuit

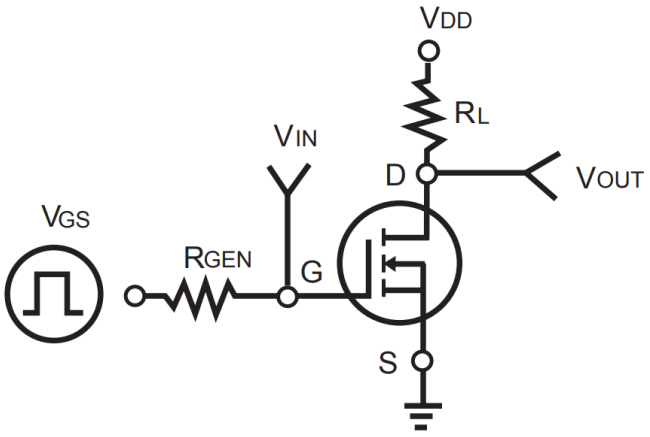
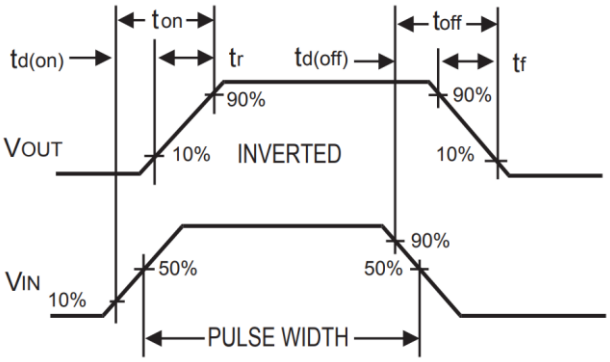


Fig. 11 ▪ Switching Waveforms



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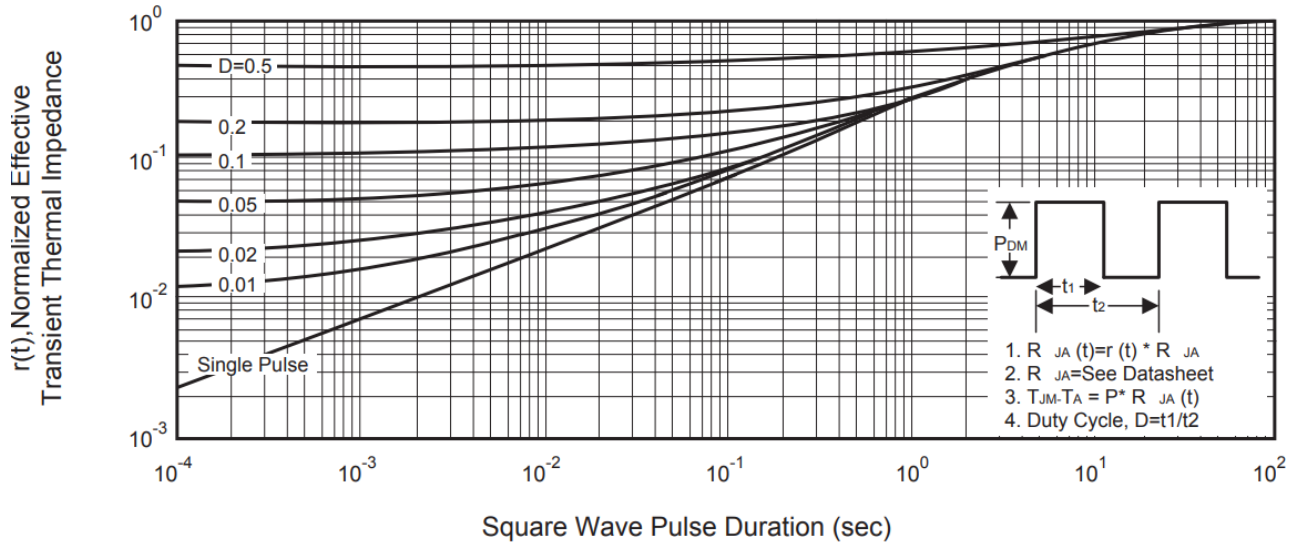
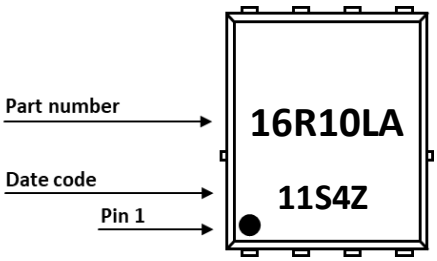
REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 12 ▪ Normalized Thermal Transient Impedance Curve

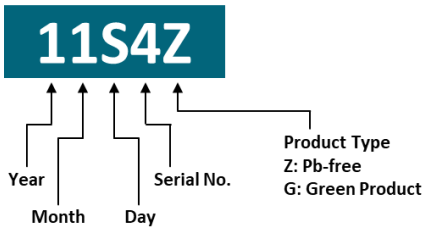


PART MARKING



DATE CODE

Example: 11S4Z



Coding list for „Day“

1	2	3	4	5	6	7	8	9	A
01	02	03	04	05	06	07	08	09	10
B	C	D	E	F	G	H	I	J	K
11	12	13	14	15	16	17	18	19	20
L	M	N	O	P	Q	R	S	T	U
21	22	23	24	25	26	27	28	29	30
V									
31									

Coding list for „Month“

1	2	3	4	5	6
Jan	Feb	Mar	Apr	May	Jun
7	8	9	A	B	C
Jul	Aug	Sep	Oct	Nov	Dec

Coding list for „Year“

0	1	2	3	4
2020	2021	2022	2023	2024
5	6	7	8	9
2025	2026	2027	2028	2029

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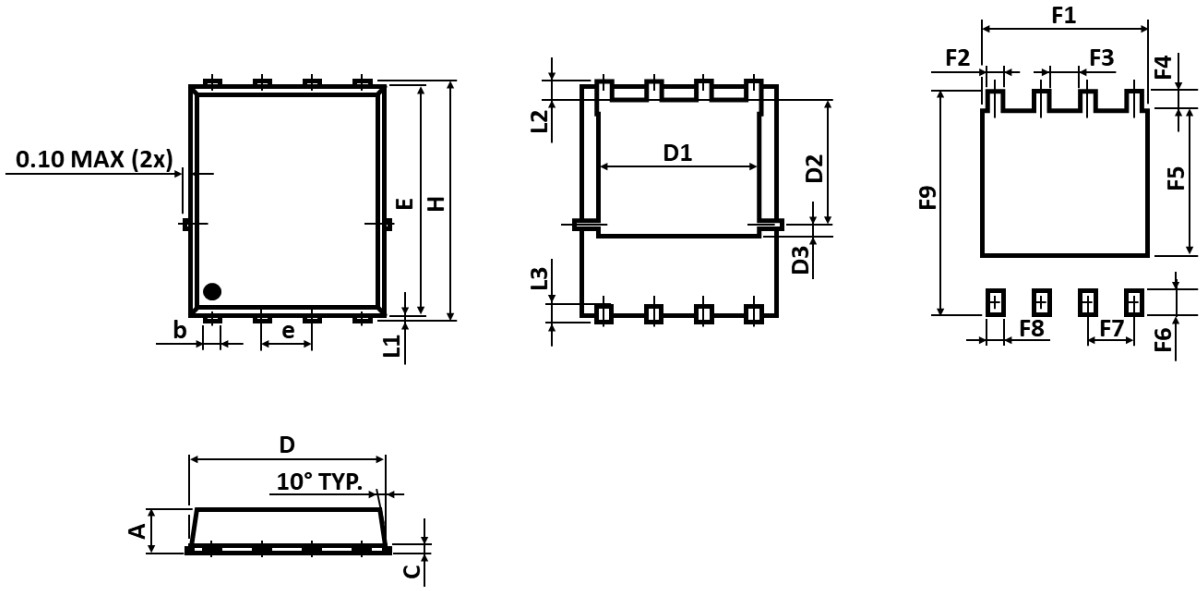
PACKAGE OUTLINE AND RECOMMENDED PAD LAYOUT



Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
A	0.800	-	1.170
b	0.340	-	0.490
c	0.200	-	0.340
D	4.800	-	5.100
D1	3.800	-	4.200
D2	3.180	-	3.780
D3	0.150	-	0.360

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
E	5.650	-	5.900
e		1.270 TYP	
H	5.900	-	6.150
L1	0.050	-	0.250
L2	0.380	-	0.620
L3	0.380	-	0.750

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F1	-	4.500	-
F2	-	0.500	-
F3	-	0.770	-
F4	-	0.550	-
F5	-	3.650	-

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F6	-	0.800	-
F7	-	1.270	-
F8	-	0.500	-
F9	-	6.250	-

Notes: **1. The suggested land pattern dimensions have been provided for reference only.**
2. For further information, please reference document IPC-7351A.

ORDERING INFORMATION

Part Number	Package	Packing	Reel Qty.	Inner Box Qty.	Outer Box Qty.
CEZ16R10LA	PPAK 5x6	Reel	2,500pcs	5,000pcs	40,000pcs

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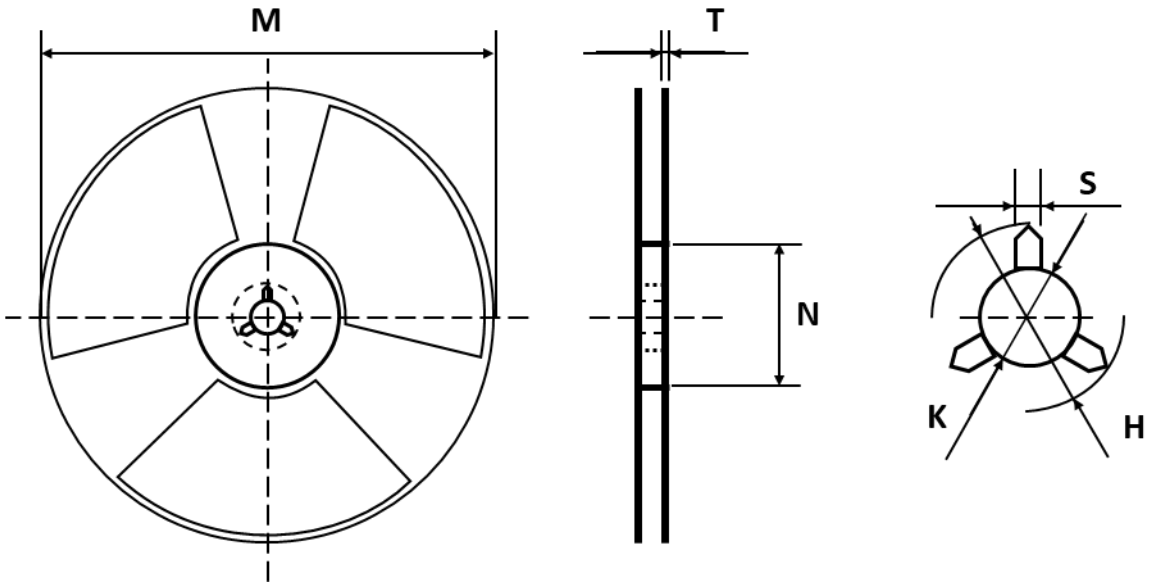
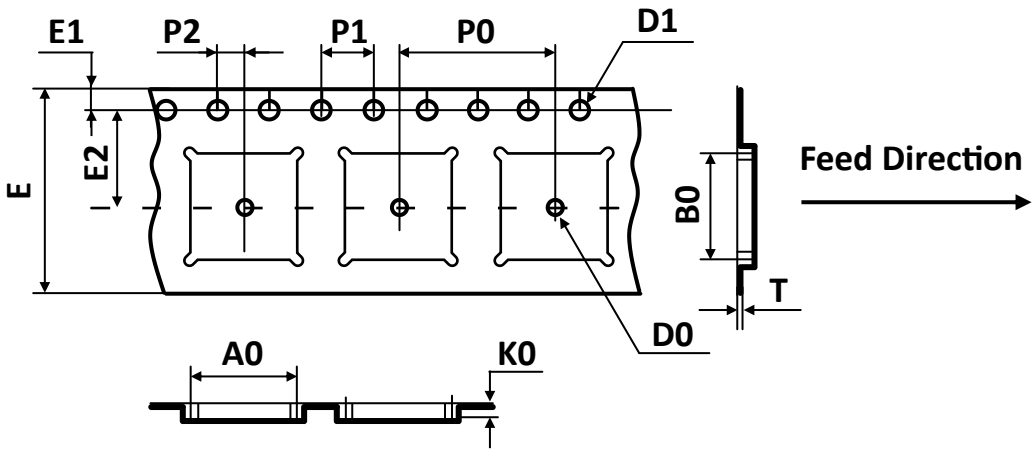
REEL DIMENSIONS ▲ All dimensions in mm



Tape Size	Reel Size	M	N	T	H	K	S
12mm	Ø330	Ø330.00	Ø100.00	2.10	22.00	13.00	2.00
		±2.00	±1.00	±0.20	±0.50	+0.50 -0.20	±0.50

TAPE DIMENSIONS ▲ All dimensions in mm



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
PPAK 5x6	6.50	5.28	2.00	1.50	1.50	12.00	1.75	5.50	8.00	4.00	2.00	0.25
	±0.10	±0.10	±0.10	±0.25	±0.10	+0.30 -0.10	±0.10	±0.05	±0.10	±0.10	±0.05	±0.02

Note: **All dimensions meet EIA-481-D requirements.**

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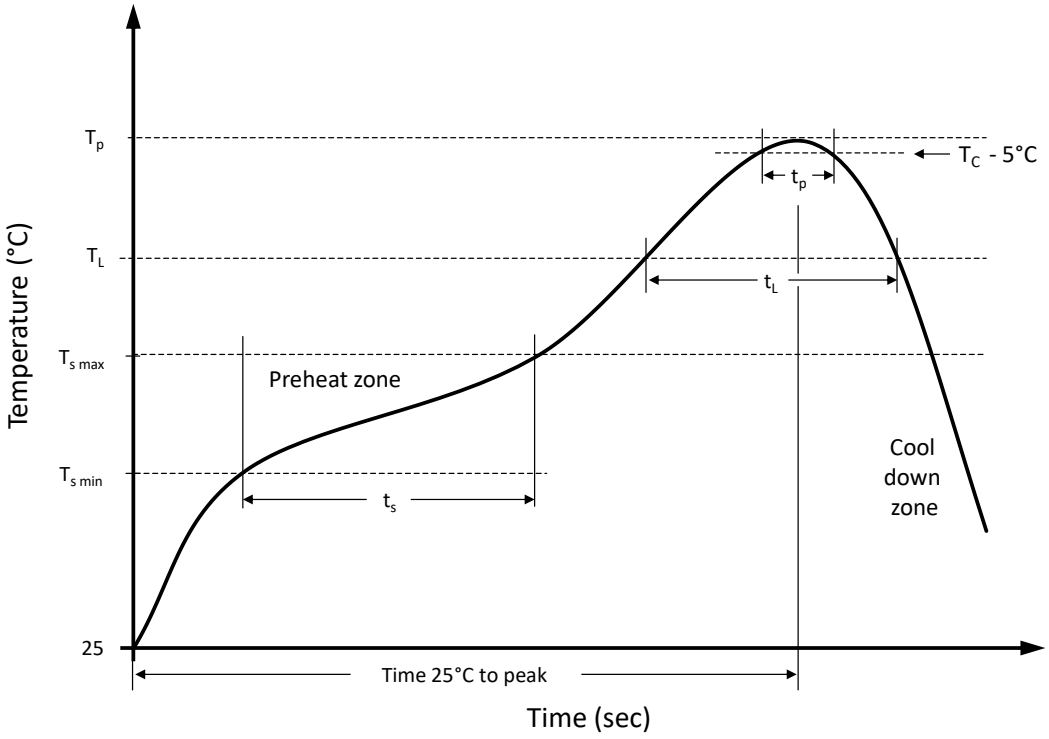
RECOMMENDED REFLOW SOLDERING PROFILE



Recommended reflow soldering conditions ▲ Refer to JEDEC J-STD-020E

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	$T_{s\,min}$	100 °C	150 °C
Preheat temperature max.	$T_{s\,max}$	150 °C	200 °C
Preheat time t_s from $T_{s\,min}$ to $T_{s\,max}$	t_s	120 seconds	120 seconds
Ramp-up rate (T_L to T_p)		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	T_L	183 °C	217 °C
Time t_L maintained above T_L	t_L	150 seconds max.	150 seconds max.
Peak package body temperature	T_p	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	t_p	20 seconds max.	30 seconds max.
Ramp-down rate (T_L to T_p)		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes

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REVISION TABLE

Revision	Date	Status	Notes
001	30/09/2022	Initial release	Initial publication

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It is subject to the user's duty of care to design and validate his products in such a way that appropriate measures are taken, such as protective circuits or redundant systems to ensure the safety standards required in the application.

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