

CEZ6515

150V ▲ 60mΩ ▲ 20A ▲ Si MOSFET

SILICON Si MOSFET ▲ SMD type

N-channel enhancement mode

UL94V-0 rated flame retardant epoxy

PPAK5x6 package ▲ MSL 3

Super high dense cell density for extremely low $R_{DS(ON)}$

High power and current handling capability

MAXIMUM RATINGS

Parameter ($T_A = 25^\circ\text{C}$, unless otherwise noted)		Characteristics
Drain-Source Voltage	V_{DS}	150V
Gate-Source Voltage	V_{GS}	$\pm 20\text{V}$
Continuous Drain Current at R_{TH_JC}	I_D	20A
Continuous Drain Current at R_{TH_JA}	I_D	7A
Pulsed Drain Current at R_{TH_JC} ^{Note 1}	I_{DM}	80A
Pulsed Drain Current at R_{TH_JA} ^{Note 1}	I_{DM}	28A
Maximum Power Dissipation	P_D	50W
Single Pulsed Avalanche Energy ^{Note 5}	E_{AS}	3.2mJ
Single Pulsed Avalanche Current ^{Note 5}	I_{AS}	8A
Operating and Storage Temperature Range	T_J, T_{STG}	-55°C to $+150^\circ\text{C}$

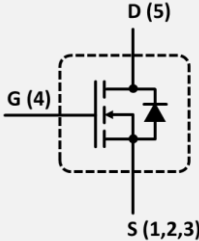
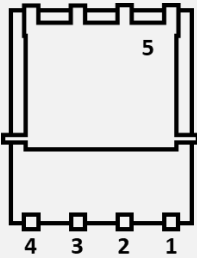
THERMAL CHARACTERISTICS

Parameter	Symbol	Limit
Thermal Resistance, Junction-to-Case	R_{TH_JC}	2.5°C/W
Thermal Resistance, Junction-to-Ambient ^{Note 2}	R_{TH_JA}	20°C/W

APPLICATIONS

Battery Management Systems	E-Bike	Industrial Control	Power Inverter	UPS
				

PIN DESCRIPTION

Circuit Diagram	Outline - Bottom View	Pin No.	Description
		1 2 3 4 5	Source Source Source Gate Drain

ELECTRICAL CHARACTERISTICS ▲ $T_A = 25^\circ\text{C}$, unless otherwise noted

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}		150		V
Zero Gate Voltage Drain Current	$V_{DS} = 135V, V_{GS} = 0V$	I_{DSS}			1	μA
Gate Body Leakage Current, Forward	$V_{GS} = 20V, V_{DS} = 0V$	I_{GSSF}			100	nA
Gate Body Leakage Current, Reverse	$V_{GS} = -20V, V_{DS} = 0V$	I_{GSSR}			-100	nA
On Characteristics ^{Note 3}						
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(th)}$	2		4	V
Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 10A$	$R_{DS(ON)}$		60	80	m Ω
Static Drain-Source On-Resistance	$V_{GS} = 6V, I_D = 5A$	$R_{DS(ON)}$		62	90	m Ω
Static Drain-Source On-Resistance	$V_{GS} = 5V, I_D = 5A$	$R_{DS(ON)}$		73	95	m Ω
Gate Input Resistance	$f = 1\text{MHz}$, Open Drain	R_G		1		Ω
Dynamic Characteristics ^{Note 4}						
Input Capacitance	$V_{DS} = 75V, V_{GS} = 0V, f = 1\text{MHz}$	C_{ISS}		1205		pF
Output Capacitance	$V_{DS} = 75V, V_{GS} = 0V, f = 1\text{MHz}$	C_{OSS}		105		pF
Reverse Transfer Capacitance	$V_{DS} = 75V, V_{GS} = 0V, f = 1\text{MHz}$	C_{RSS}		50		pF
Switching Characteristics ^{Note 4}						
Turn-On Delay Time	$V_{DD} = 75V, V_{GS} = 10V, I_D = 10A, R_{G(ext)} = 6\Omega$	$t_{D(ON)}$		19		ns
Turn-On Rise Time	$V_{DD} = 75V, V_{GS} = 10V, I_D = 10A, R_{G(ext)} = 6\Omega$	t_R		8		ns
Turn-Off Delay Time	$V_{DD} = 75V, V_{GS} = 10V, I_D = 10A, R_{G(ext)} = 6\Omega$	$t_{D(OFF)}$		33		ns
Turn-Off Fall Time	$V_{DD} = 75V, V_{GS} = 10V, I_D = 10A, R_{G(ext)} = 6\Omega$	t_F		6		ns
Total Gate Charge	$V_{DS} = 75V, V_{GS} = 10V, I_D = 10A$	Q_G		27		nC
Gate Source Charge	$V_{DS} = 75V, V_{GS} = 10V, I_D = 10A$	Q_{GS}		5		nC
Gate Drain Charge	$V_{DS} = 75V, V_{GS} = 10V, I_D = 10A$	Q_{GD}		10		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^{Note3}		I_S			20	A
Drain-Source Diode Forward Voltage ^{Note3}	$V_{GS} = 0V, I_S = 10A$	V_{SD}			1.2	V

Notes

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: Surface Mounted on FR4 Board, $t \leq 10$ sec
- 3: Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- 4: Guaranteed by design, not subject to production testing.
- 5: $L = 0.1\text{mH}$, $I_{AS} = 8A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 1 • Output Characteristics

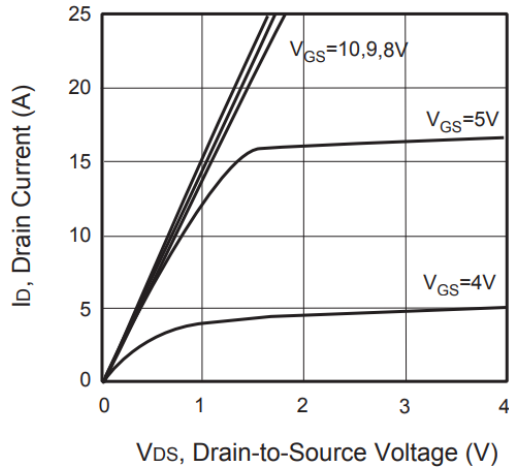


Fig. 2 • Transfer Characteristics

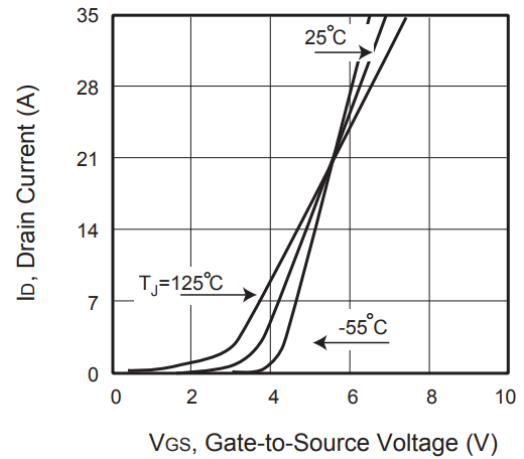


Fig. 3 • Capacitance

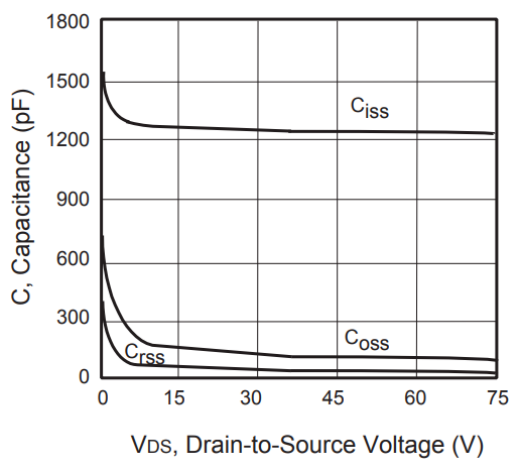


Fig. 4 • On-Resistance Variation with Temperature

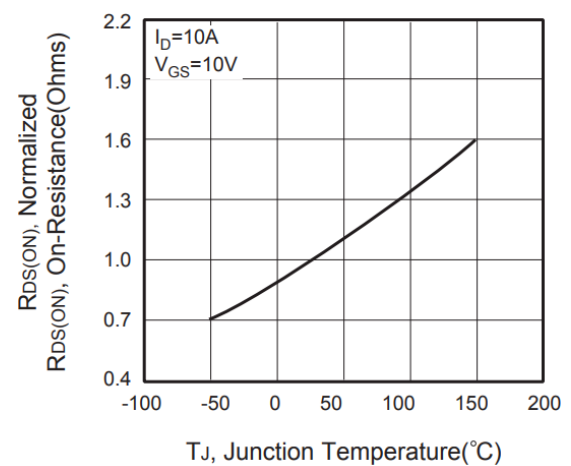


Fig. 5 • Gate Threshold Variation with Temperature

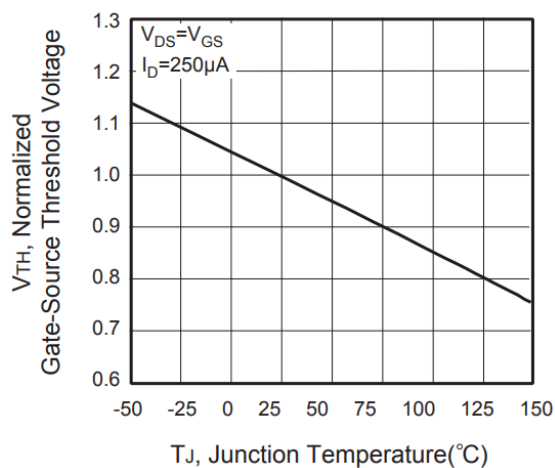
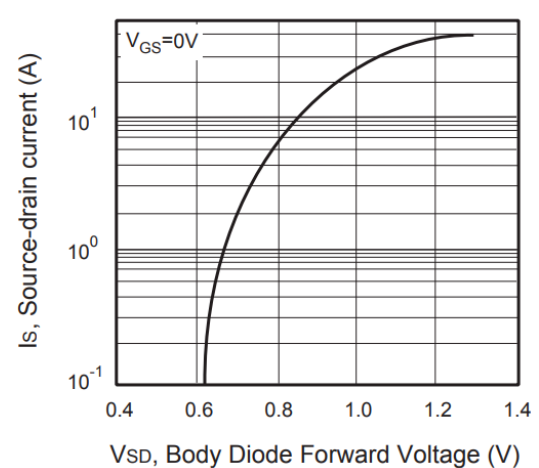


Fig. 6 • Body Diode Forward Voltage Variation with Source Current



REFERENCE DATA ▲ TYPICAL DEVICE PERFORMANCE

Fig. 7 • Gate Charge

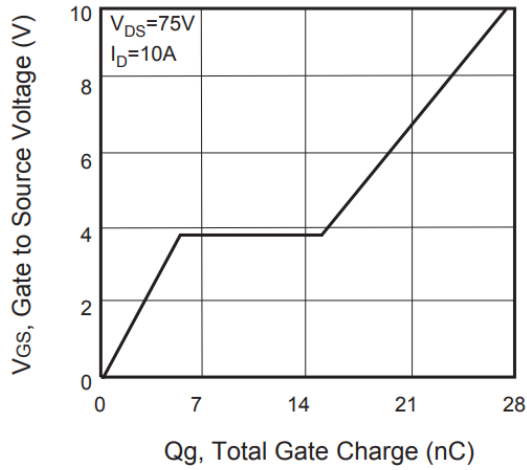


Fig. 8 • Maximum Safe Operating Area

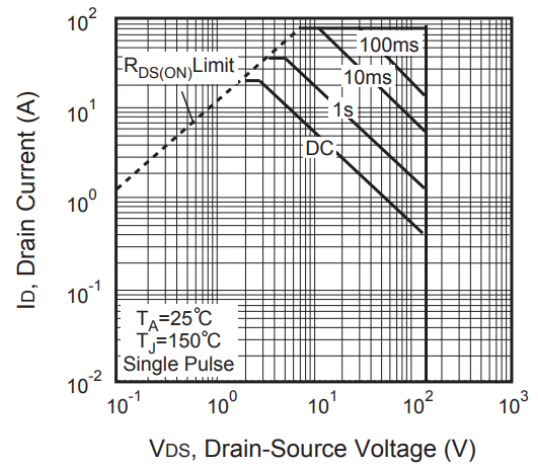


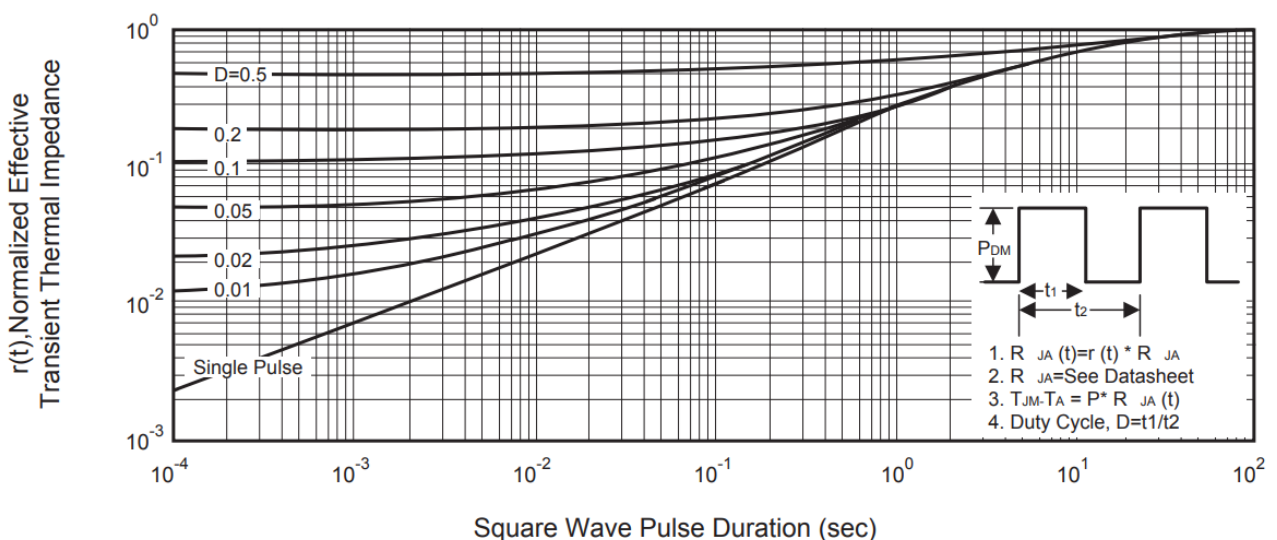
Fig. 9 • Switching Test Circuit



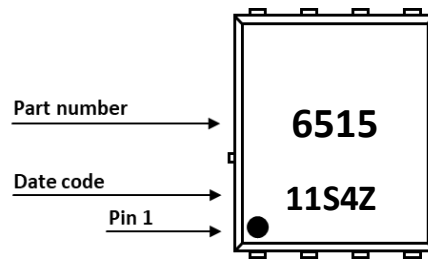
Fig. 10 • Switching Waveforms



Fig. 11 • Normalized Thermal Transient Impedance Curve



PART MARKING



DATE CODE

Example: 11S4Z



Coding list for „Day“

1	2	3	4	5	6	7	8	9	A
01	02	03	04	05	06	07	08	09	10
B	C	D	E	F	G	H	I	J	K
11	12	13	14	15	16	17	18	19	20
L	M	N	O	P	Q	R	S	T	U
21	22	23	24	25	26	27	28	29	30
V									
31									

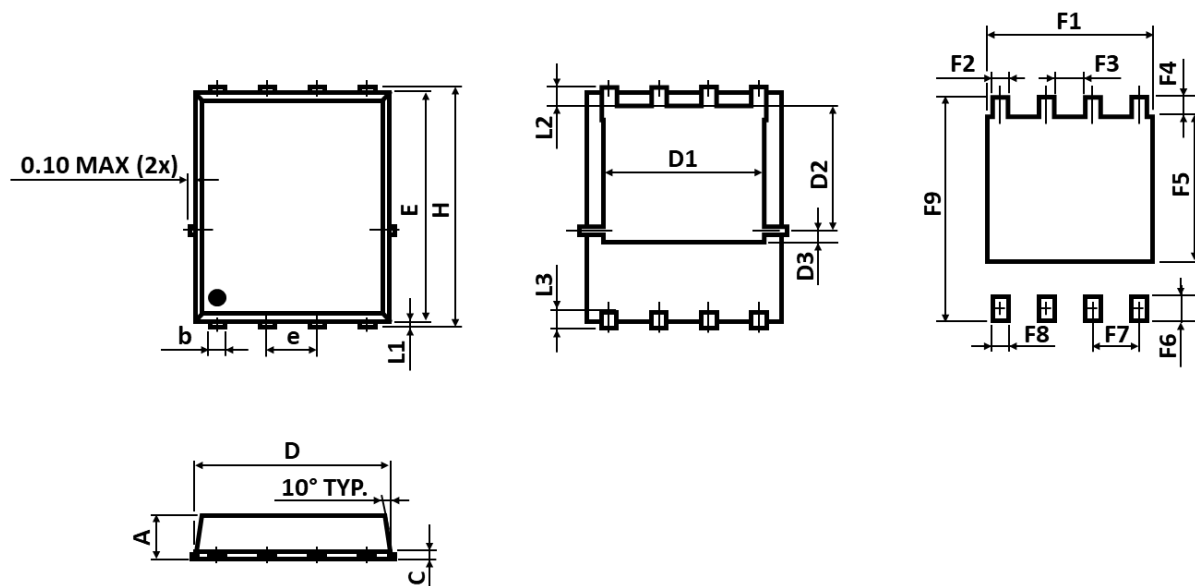
Coding list for „Month“

1	2	3	4	5	6
Jan	Feb	Mar	Apr	May	Jun
7	8	9	A	B	C
Jul	Aug	Sep	Oct	Nov	Dec

Coding list for „Year“

0	1	2	3	4
2020	2021	2022	2023	2024
5	6	7	8	9
2025	2026	2027	2028	2029

PACKAGE OUTLINE AND RECOMMENDED PAD LAYOUT



Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
A	0.800	-	1.170
b	0.340	-	0.490
c	0.200	-	0.340
D	4.800	-	5.100
D1	3.800	-	4.200
D2	3.180	-	3.780
D3	0.150	-	0.360

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
E	5.650	-	5.900
e	1.270 TYP		
H	5.900	-	6.150
L1	0.050	-	0.250
L2	0.380	-	0.620
L3	0.380	-	0.750

Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F1	-	4.500	-
F2	-	0.500	-
F3	-	0.770	-
F4	-	0.550	-
F5	-	3.650	-

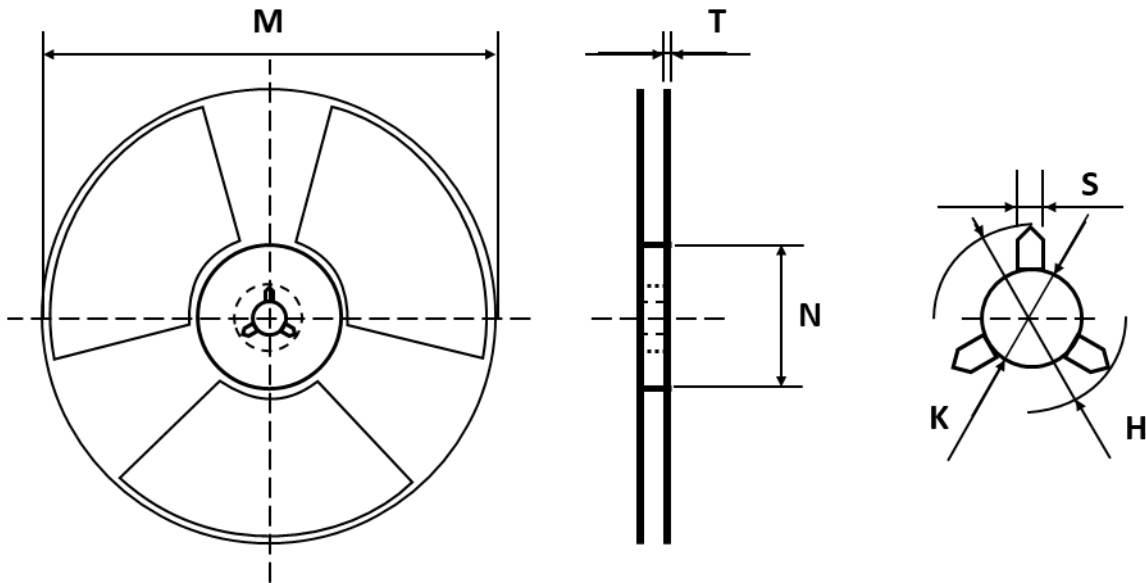
Sym	Millimeters (Min.)	Millimeters (Typ.)	Millimeters (Max.)
F6	-	0.800	-
F7	-	1.270	-
F8	-	0.500	-
F9	-	6.250	-

- Notes: 1. The suggested land pattern dimensions have been provided for reference only.
2. For further information, please reference document IPC-7351A.

ORDERING INFORMATION

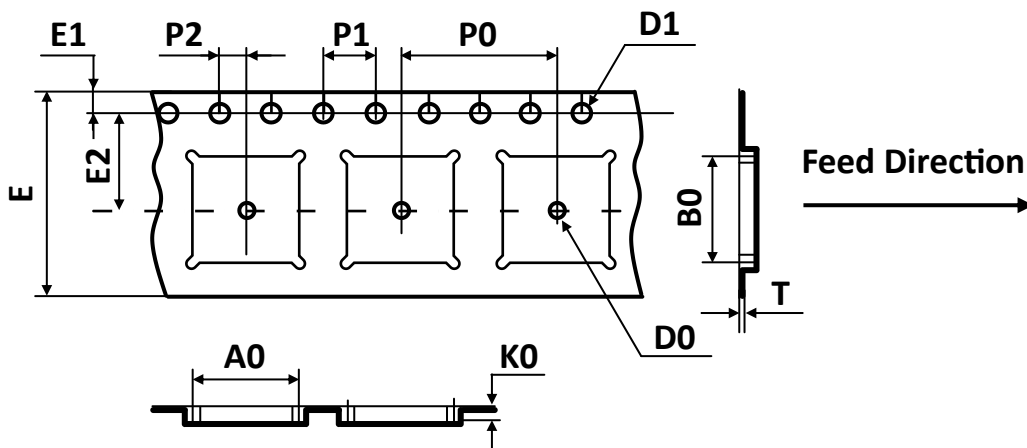
Part Number	Package	Packing	Reel Qty.	Inner Box Qty.	Outer Box Qty.
CEZ6515	PPAK 5x6	Reel	2,500pcs	5,000pcs	40,000pcs

REEL DIMENSIONS ▲ All dimensions in mm



Tape Size	Reel Size	M	N	T	H	K	S
12mm	Ø330	Ø330.00	Ø100.00	2.10	22.00	13.00	2.00
		±2.00	±1.00	±0.20	±0.50	+0.50 -0.20	±0.50

TAPE DIMENSIONS ▲ All dimensions in mm



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
PPAK 5x6	6.50	5.28	2.00	1.50	1.50	12.00	1.75	5.50	8.00	4.00	2.00	0.25
	±0.10	±0.10	±0.10	±0.25	±0.10	+0.30 -0.10	±0.10	±0.05	±0.10	±0.10	±0.05	±0.02

Note: All dimensions meet EIA-481-D requirements.

RECOMMENDED REFLOW SOLDERING PROFILE



Recommended reflow soldering conditions ▲ Refer to JEDEC J-STD-020E

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	$T_{s \text{ min}}$	100 °C	150 °C
Preheat temperature max.	$T_{s \text{ max}}$	150 °C	200 °C
Preheat time t_s from $T_{s \text{ min}}$ to $T_{s \text{ max}}$	t_s	120 seconds	120 seconds
Ramp-up rate (T_L to T_p)		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	T_L	183 °C	217 °C
Time t_L maintained above T_L	t_L	150 seconds max.	150 seconds max.
Peak package body temperature	T_p	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	t_p	20 seconds max.	30 seconds max.
Ramp-down rate (T_L to T_p)		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes

REVISION TABLE

Revision	Date	Status	Notes
001	30/09/2022	Initial release	Initial publication

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