

GPT65C0YME

650V ▲ 230mΩ ▲ GaN FET
GALLIUM NITRIDE GaN FET ▲ SMD type

Normally off device

Easy to drive with standard MOSFET driver

Small size in 8mm x 8mm ▲ DFN8080 package

Moisture Sensitivity Level ▲ MSL 3

Ultra-low Q_{RR} and very robust design

SPECIFICATION

Item ($T_c = 25^\circ\text{C}$, unless otherwise noted)		Characteristics
Operating Temperature Range	T_J	-55°C to $+150^\circ\text{C}$
Storage Temperature Range	T_S	-55°C to $+150^\circ\text{C}$
Drain-Source Voltage	V_{DSS}	650V
Transient Drain-Source Voltage ^{Note 1}	$V_{TR(DSS)}$	800V
Drain-Source On-State Resistance ^{Note 2}	$R_{DS(ON)TYP}$	230mΩ
Typical Recovered Charge ^{Note 3}	Q_{RR}	18.6nC
Typical Total Gate Charge	Q_G	16nC

Notes

- 1: Spike duty cycle $DC < 0.01$, spike duration time $< 20\mu\text{s}$ during off-state mode
- 2: $V_{GS} = 10\text{V}$, $I_{DS} = 6\text{A}$
- 3: See diode reverse recovery test circuit and waveform, Fig. 15, and Fig. 16

APPLICATIONS

Battery Chargers	Power Adapters	LED Lighting	Wireless Power	AC/DC Converter	DC/DC Converter	Class D Audio Amplifiers

PIN DESCRIPTION

Circuit Diagram	Outline - Bottom View	Pin No.	Symbol	Description
		1 2 3	G D S	Gate Drain Source

STORAGE AND HANDLING CONDITIONS

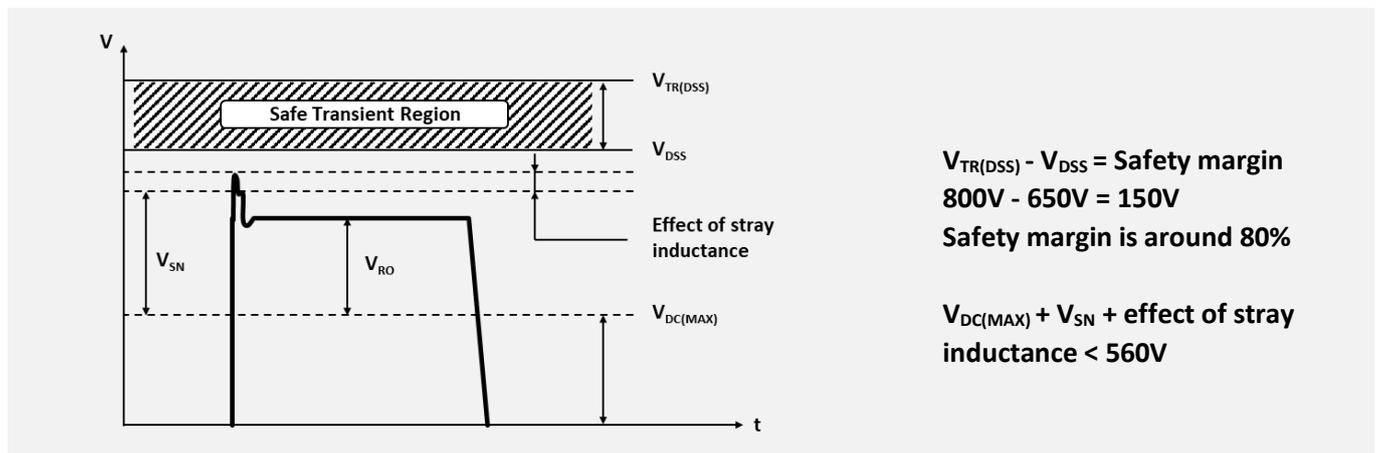
ESD level	Floor life	Conditions	MSL
HBM class 2	168 hours	$T_A < 30^\circ\text{C}$, RH < 60%	3

ABSOLUTE MAXIMUM RATINGS ▲ $T_C = 25^\circ\text{C}$, unless otherwise noted

Item	Condition	Symbol	Limit	Unit
Drain-Source Breakdown Voltage		V_{DSS}	650	V
Transient Drain-Source Voltage ^{Note1}		$V_{(TR)DSS}$	800	V
Gate-Source Voltage		V_{GSS}	±18	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$ ^{Note 2}	I_D	6	A
Continuous Drain Current	$T_C = 100^\circ\text{C}$ ^{Note 2}	I_D	3.9	A
Pulse Drain Current	Pulse Width = 10µs	I_{DM}	27	A
Operating Temperature Range	Case	T_C	-55 to +150	°C
Operating Temperature Range	Junction	T_J	-55 to +150	°C
Storage Temperature Range		T_S	-55 to +150	°C

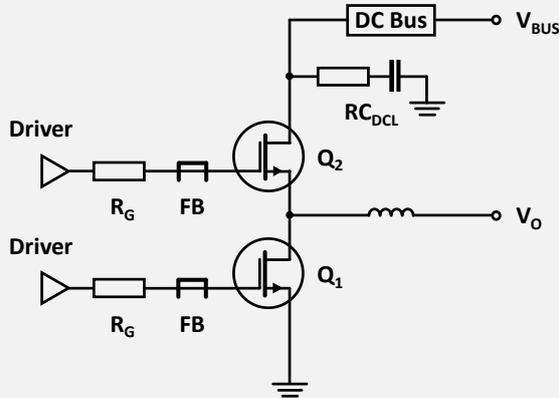
Note:

- 1: Spike duty cycle DC < 0.01, spike duration time < 20µs during off-state mode
- 2: See application information for increased stability at high current operation, fig. 2

Fig. 1 • Voltage Stress Primary Switch with 264VAC


$V_{DC(MAX)}$	Maximum input voltage
V_{RO}	Reflected output voltage
V_{SN}	Snubber capacitor voltage
V_{DSS}	Drain-Source breakdown voltage
$V_{(TR)DSS}$	Transient Drain-source voltage

APPLICATION INFORMATION

Fig. 2 ▪ Recommended Circuit for Improved Stability at High Current Operation


A ferrite bead (FB) should be connected in series with the gate pin to dampen the resonant circuit of gate-source loop inductance and the input capacitance of the GaN-FET. The ferrite bead should be placed as close as possible to the gate pin to minimize the gate-source loop. (See figure 2). This causes fast switching stability. We recommend an impedance of 240Ω at 100MHz for the ferrite bead. In addition, a series resistance (R_G) of 10 to 15Ω should be provided.

Furthermore, a DC-link snubber should always be used to eliminate instability of the GaN-FET. In the simplest case, an RC combination is connected in parallel to the DC link bus, which significantly reduces the Q factor of any resonance in the bus. We recommend an MLCC between 4.7 and 10nF and an SMD resistor with 5.1Ω as well-suited values.

THERMAL CHARACTERISTIC RATINGS

Items		Typ.
Thermal Resistance Junction to Ambient ^{Note 1}	R_{thJA}	53°C/W
Thermal Resistance Junction to Case	R_{thJC}	1°C/W

Note:

- 1: Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper and 70μm thickness)

ELECTRICAL CHARACTERISTICS ▲ $T_C = 25^\circ\text{C}$, unless otherwise noted

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$	V_{DSS}	650			V
Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 500\mu\text{A}$	V_{GSth}	1	1.7	2.5	V
Gate-Source Leakage Current	$V_{GS} = 18\text{V}, V_{DS} = 0\text{V}$	I_{GSS}			100	nA
Gate-Source Leakage Current	$V_{GS} = -18\text{V}, V_{DS} = 0\text{V}$	I_{GSS}			-100	nA
Drain-Source Leakage Current	$V_{DS} = 650\text{V}, V_{GS} = 0\text{V}$	I_{DSS}		5	10	μA
Drain-Source Leakage Current	$V_{DS} = 650\text{V}, V_{GS} = 0\text{V}, T_J = 150^\circ\text{C}$	I_{DSS}		15		μA
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_{DS} = 6\text{A}$	$R_{DS(ON)}$		230	300	m Ω
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_{DS} = 6\text{A}, T_J = 150^\circ\text{C}$	$R_{DS(ON)}$		405		m Ω

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Dynamic Characteristics						
Input Capacitance	$V_{DS} = 400\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{ISS}		400		pF
Output Capacitance	$V_{DS} = 400\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{OSS}		40		pF
Reverse Transfer Capacitance	$V_{DS} = 400\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{RSS}		8		pF
Effective Output Capacitance, Energy Related ^{Note 1}	$V_{DS} = 0 \text{ to } 400\text{V}, V_{GS} = 0\text{V}$	$C_{O(ER)}$		175		pF
Effective Output Capacitance, Time Related ^{Note 2}	$V_{DS} = 0 \text{ to } 400\text{V}, V_{GS} = 0\text{V}$	$C_{O(TR)}$		116		pF
Total Gate Charge	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 4\text{A}$	Q_G		16		nC
Gate-Source Charge	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 4\text{A}$	Q_{GS}		2.8		nC
Gate-Drain Charge	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 4\text{A}$	Q_{GD}		4.1		nC
Output Charge	$V_{DS} = 0 \sim 400\text{V}, V_{GS} = 0\text{V}$	Q_{OSS}		46		nC
Turn-On Delay	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 6\text{A}, R_G = 30\Omega$	$t_{D(ON)}$		8		ns
Rise Time	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 6\text{A}, R_G = 30\Omega$	t_R		4		ns
Turn-Off Delay	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 6\text{A}, R_G = 30\Omega$	$t_{D(OFF)}$		17		ns
Fall Time	$V_{DS} = 400\text{V}, V_{GS} = 0 \text{ to } 8\text{V}, I_D = 6\text{A}, R_G = 30\Omega$	t_F		8		ns

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Source-Drain Diode						
Reverse Current	$V_{GS} = 0\text{V}$	I_S			6	A
Source-Drain Voltage	$I_S = 3\text{A}, V_{GS} = 0\text{V}$	V_{SD}		1.4		V
	$I_S = 6\text{A}, V_{GS} = 0\text{V}$			2.4		V
Reverse Recovery Time ^{Note 3}	$I_S = 4\text{A}, V_{DS} = 400\text{V}, di/dt = 200\text{A}/\mu\text{s}$	t_{RR}		11		ns
Recovered Charge ^{Note 4}	$I_S = 4\text{A}, V_{DS} = 400\text{V}, di/dt = 200\text{A}/\mu\text{s}$	Q_{RR}		18.6		nC

Notes:

- 1: Equivalent capacitance to give same stored energy from 0V to the stated V_{DS}
- 2: Equivalent capacitance to give same charging time from 0V to the stated V_{DS}
- 3: See diode reverse recovery test circuit and waveform, fig. 15 and fig 16
- 4: See diode reverse recovery test circuit and waveform, fig 15 and fig. 16

REFERENCE DATA

Fig. 3 • Typ. Output Characteristics I_D vs. V_{DS} , $T_J = 25^\circ\text{C}$

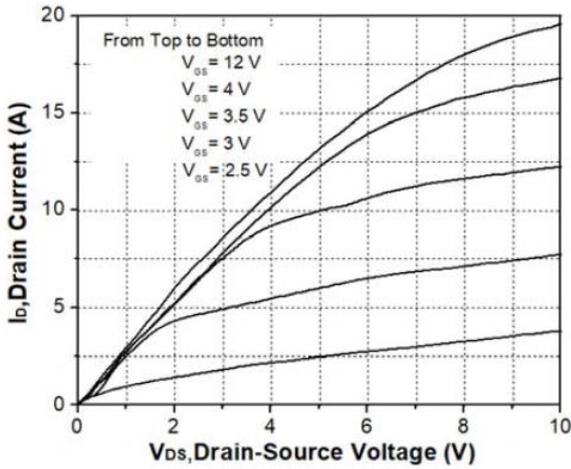


Fig. 4 • Typ. Output Characteristics I_D vs. V_{DS} , $T_J = 150^\circ\text{C}$

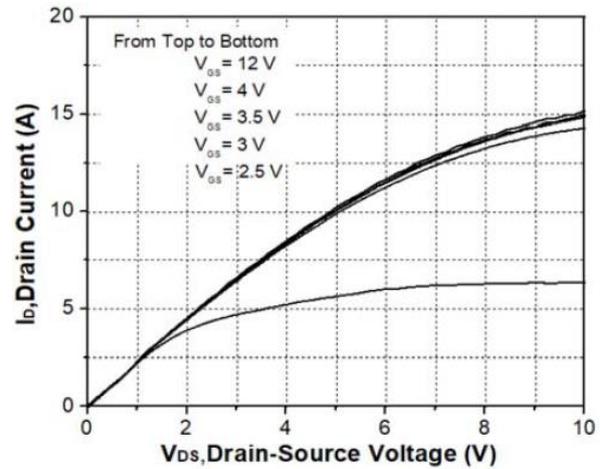


Fig. 5 • Typ. Transfer Characteristics I_D vs. V_{GS} , $V_{DS} = 10\text{ V}$

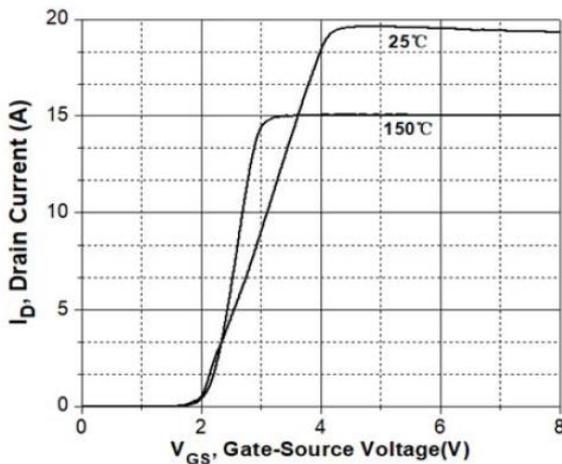


Fig. 6 • Normalized $R_{DS(ON)}$ Characteristics, $I_D = 6\text{ A}$, $V_{GS} = 10\text{ V}$

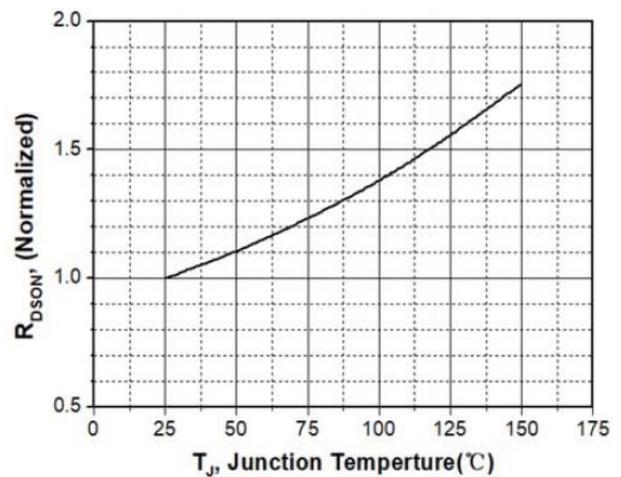


Fig. 7 • Typ. Capacitance Characteristics, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$

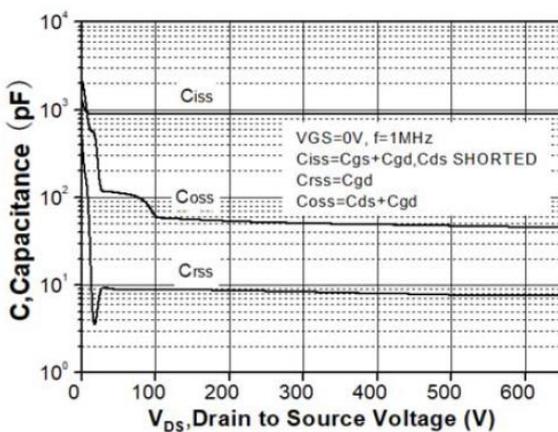
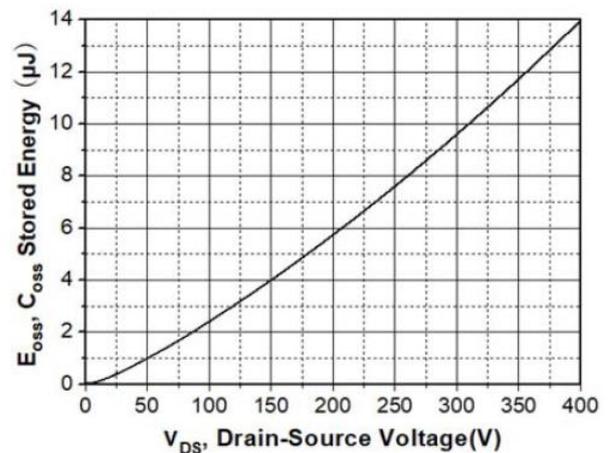


Fig. 8 • Typ. Stored Energy Characteristics C_{oss}



REFERENCE DATA

Fig. 9 • Typ. Capacitance Charge Characteristics

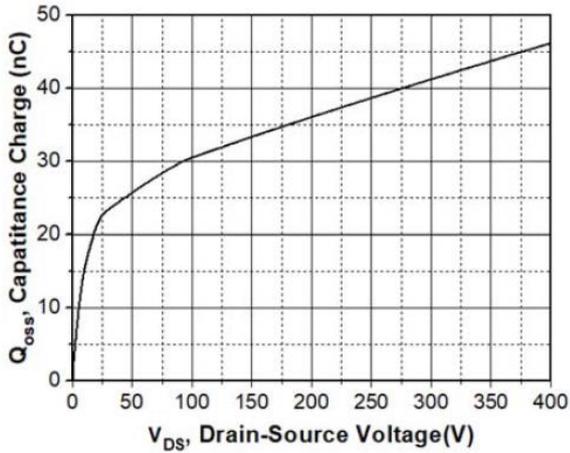


Fig. 10 • Typ. Gate Charge Characteristics, $I_D = 4A, V_{DS} = 400V$

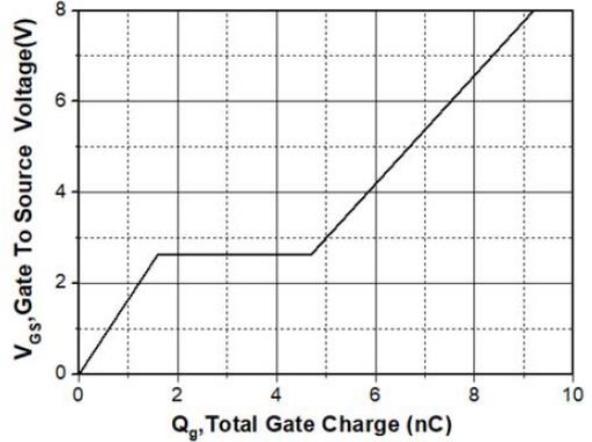


Fig. 11 • Forward Characteristics of Reverse Diode $I_S = f(V_{SD})$

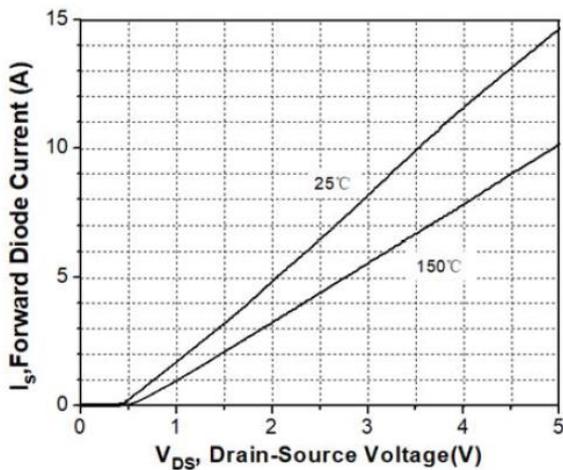


Fig. 12 • Safe Operating Area, $T_C = 25^\circ C$ (calculated based on thermal limit)

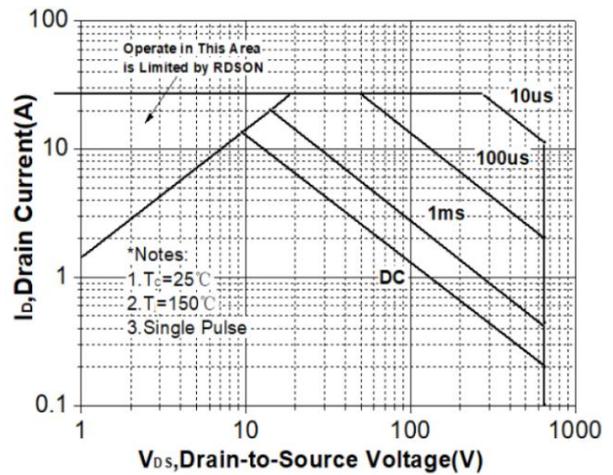


Fig. 13 • Power Dissipation vs. Case Temperature T_C

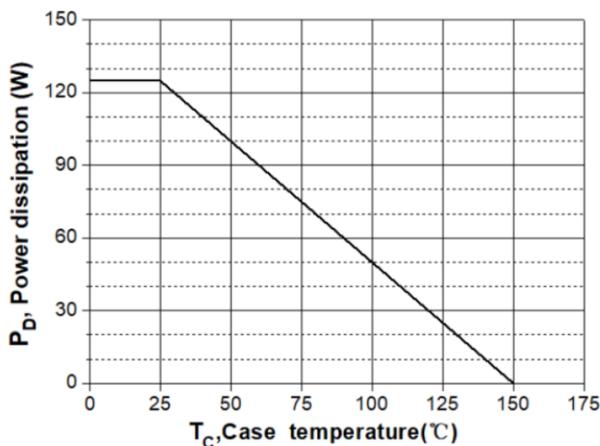
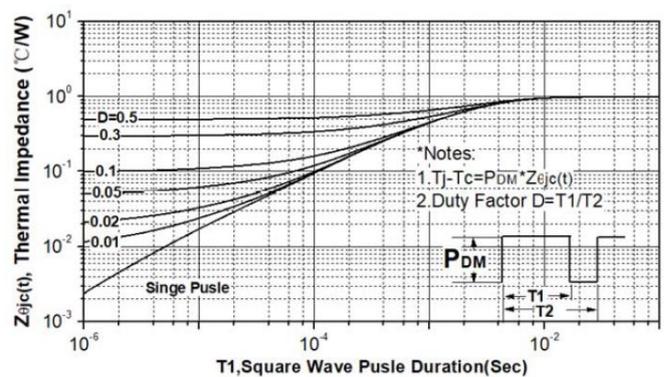


Fig. 14 • Transient thermal impedance R_{thJC}



TEST CIRCUITS AND WAVEFORMS

Fig. 15 • Diode reverse recovery test circuit

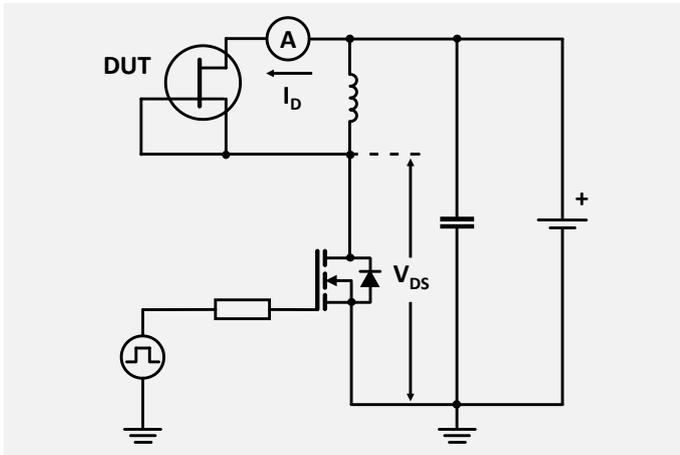


Fig. 16 • Diode reverse recovery waveform

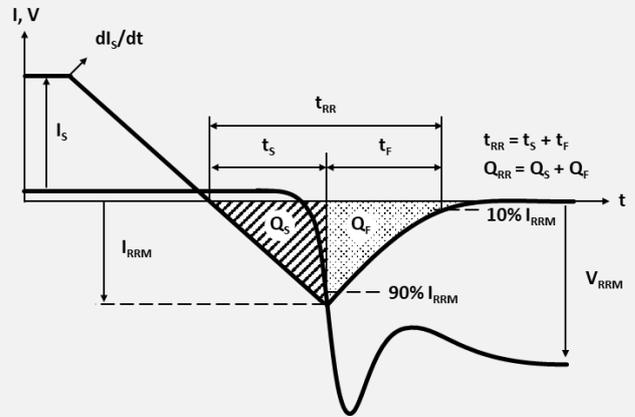


Fig. 17 • Switching time test circuit

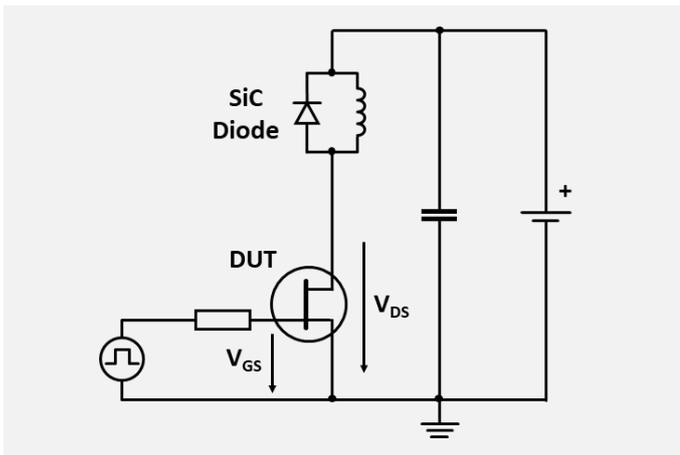


Fig. 18 • Switching time waveform

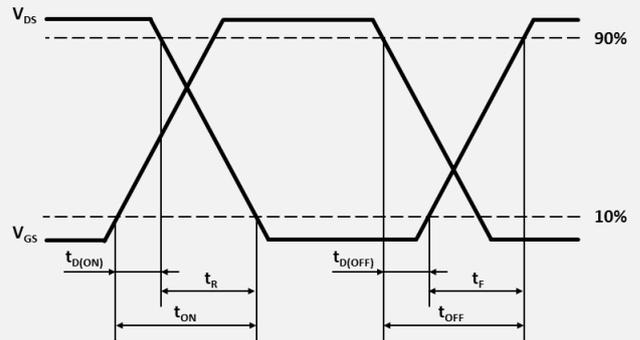


Fig. 19 • Dynamic $R_{DS(ON)eff}$ test circuit

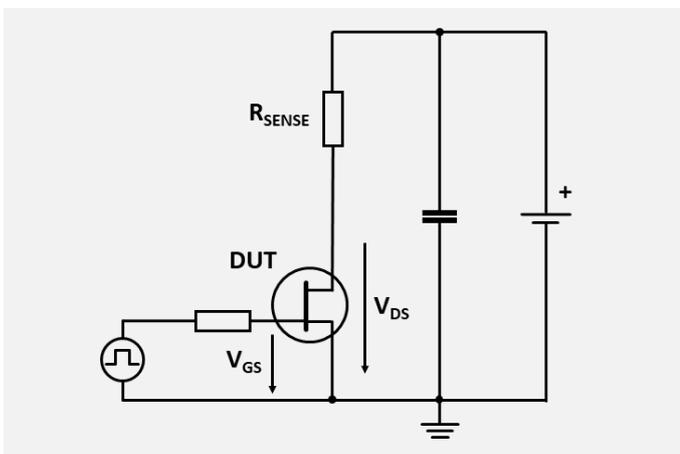
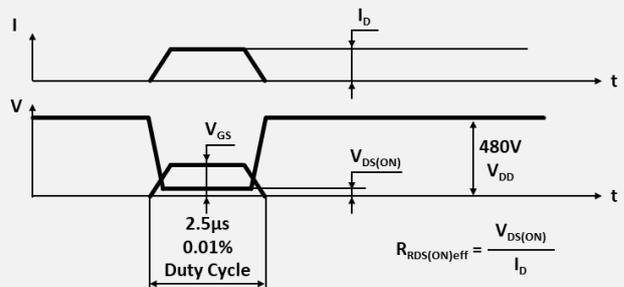
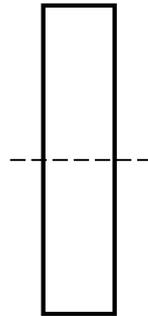
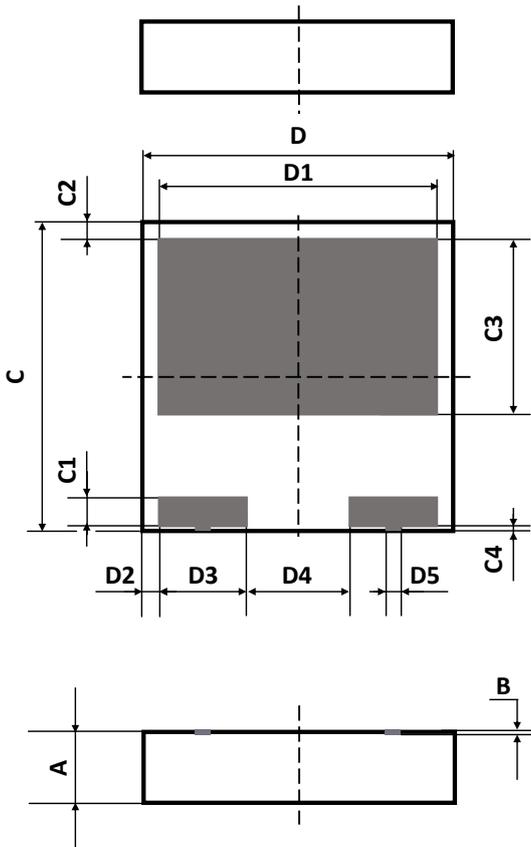


Fig. 20 • Dynamic $R_{DS(ON)eff}$ waveform



PACKAGE OUTLINE AND PART MARKING



Part number →
Date code →
Pin 1 - Gate →



Date code:

09: e.g., week 09

16: e.g., 2022

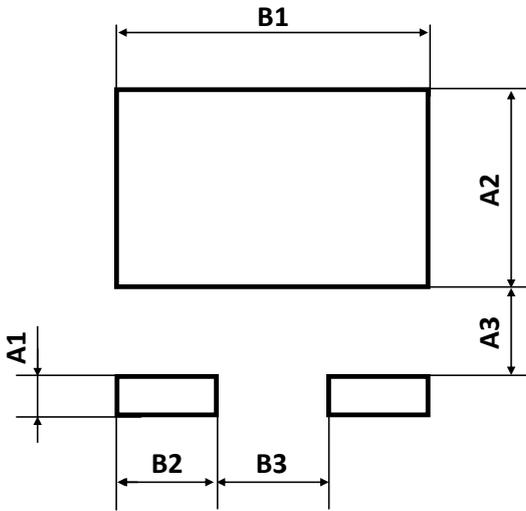
Sym	Millimeters
A	1.850 ± 0.025
B	0.203 ± 0.008
C	8.000 ± 0.050
C1	0.800 ± 0.025
C2	0.400 ± 0.025
C3	4.600 ± 0.050
C4	0.100 ± 0.025

Sym	Millimeters
D	8.000 ± 0.050
D1	7.200 ± 0.050
D2	0.400 ± 0.025
D3	2.300 ± 0.025
D4	2.600 ± 0.025
D5	0.400 ± 0.025

DATE CODE

Example: 0916

09		16	
Week of the Month		Year	
01	1 st	16	2022
02	2 nd	17	2023
03	3 rd	18	2024
04	4 th	19	2025
04	4 th	1A	2026
...	...	1B	2026
52	52 nd
		1F	2031

RECOMMENDED PAD LAYOUT FOR DFN 8080


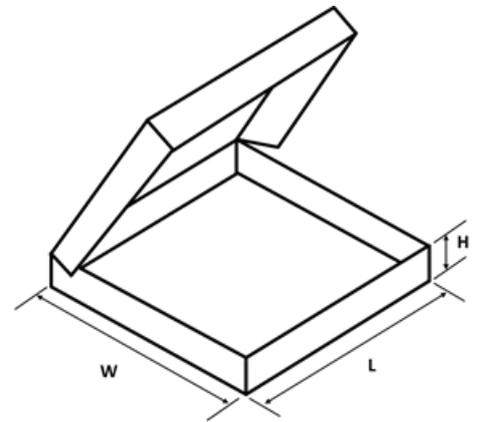
Sym	Millimeters
A1	1.000
A2	4.750
A3	2.000
B1	7.350
B2	2.450
B3	2.450

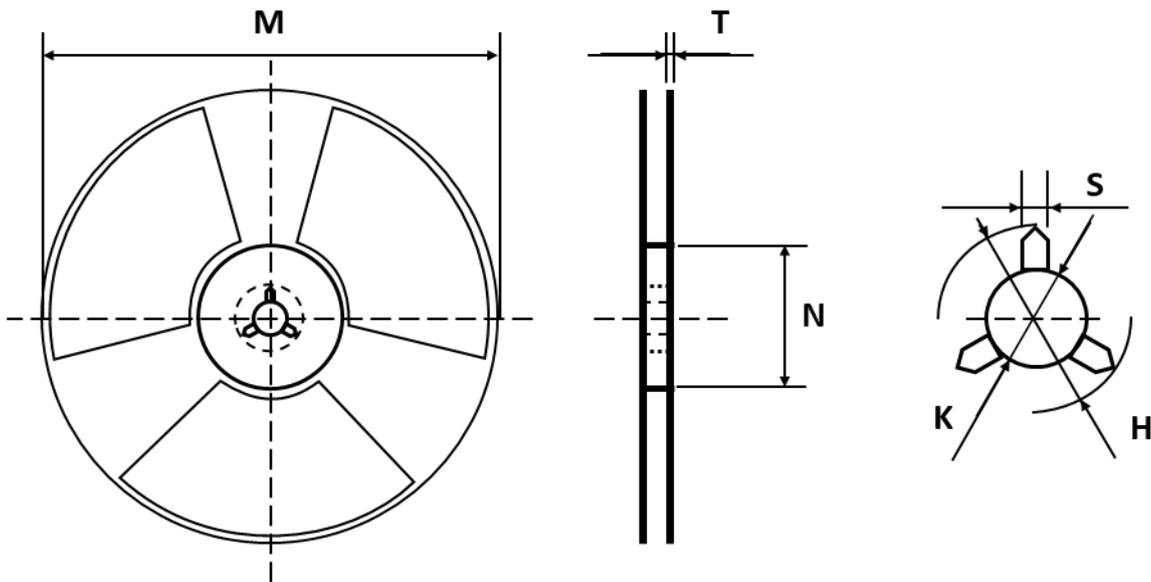
ORDERING INFORMATION

Part Number	Package	Packing	Quantity	Reel Diameter
GPT65C0YME	DFN8080	Tape and Reel	2500pcs	330mm (13")

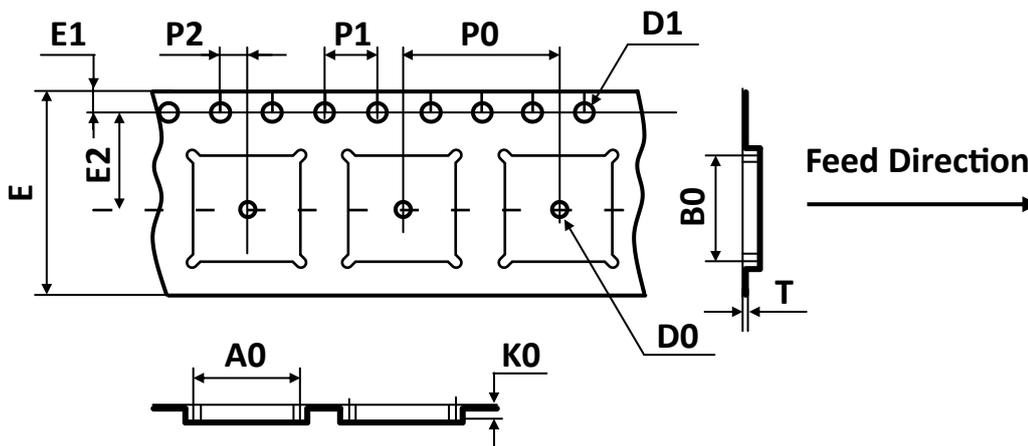
REEL BOX DIMENSION ▲ All dimensions in mm

Outside Dimensions	
Ø 330mm reel	
W	350
L	350
H	80



REEL DIMENSIONS ▲ All dimensions in mm


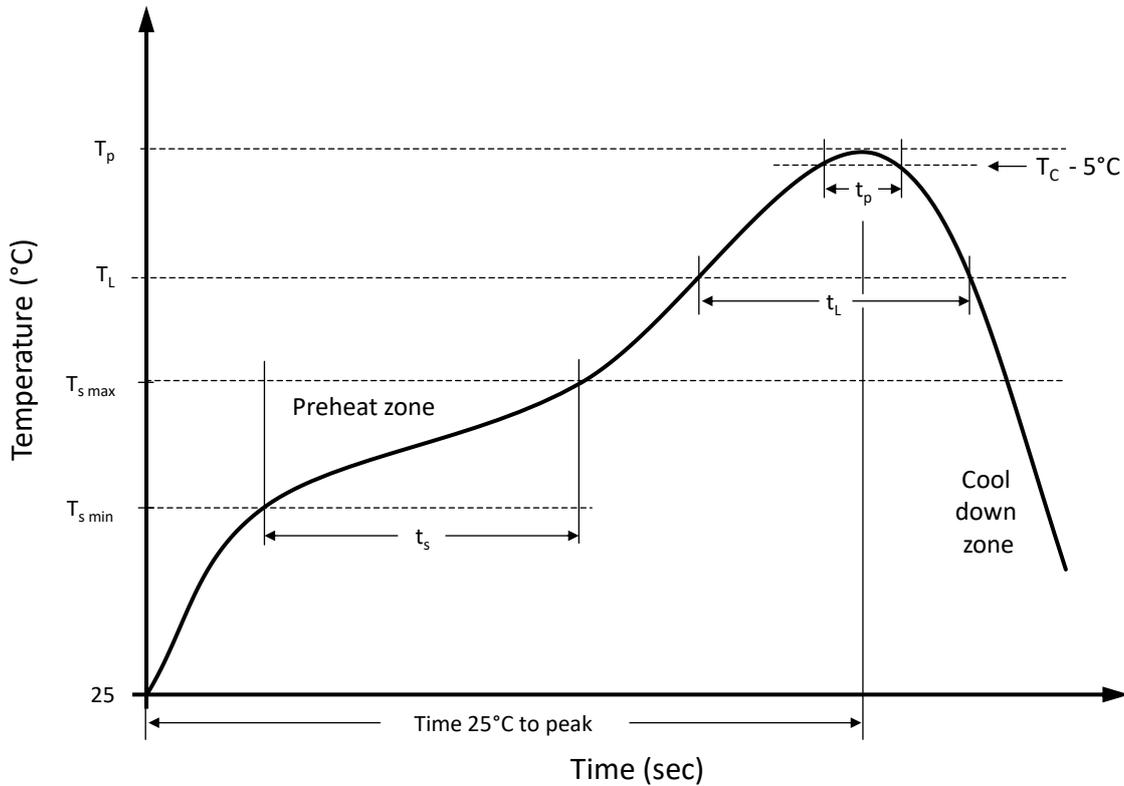
Tape Size	Reel Size	M	N	T	H	K	S
24mm	Ø330	Ø330.00	Ø102.00	2.00	13.00	10.50	2.00
		±0.20	±0.10	±2.0	+0.50 -0.20	±0.25	±0.25

TAPE DIMENSIONS ▲ All dimensions in mm


Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN8080	8.30	8.30	1.15	1.50	1.50	24.00	1.75	7.50	12.00	4.00	2.00	0.30
	±0.10	±0.10	±0.10	±0.10	±0.10	±0.30	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05

Note: All dimensions meet EIA-481-D requirements.

RECOMMENDED REFLOW SOLDERING PROFILE



Recommended reflow soldering conditions ▲ Refer to JEDEC J-STD-020E

Profile Features		Sn-Pb Eutetic Assembly	Pb-Free Assembly
Preheat temperature min.	$T_{s \text{ min}}$	100 °C	150 °C
Preheat temperature max.	$T_{s \text{ max}}$	150 °C	200 °C
Preheat time t_s from $T_{s \text{ min}}$ to $T_{s \text{ max}}$	t_s	120 seconds	120 seconds
Ramp-up rate (T_L to T_p)		max. 3 °C/second	max. 3 °C/second
Liquidous temperature	T_L	183 °C	217 °C
Time t_L maintained above T_L	t_L	150 seconds max.	150 seconds max.
Peak package body temperature	T_p	235°C	260°C
Timeframe of within 5°C below and up to max actual peak body temperature	t_p	20 seconds max.	30 seconds max.
Ramp-down rate (T_L to T_p)		max. 6 °C/second	max. 6 °C/second
Time 25°C to peak temperature		max. 6 minutes	max. 8 minutes

REVISION TABLE

Revision	Date	Status	Notes
001	01/01/2022	Initial release	Initial publication
002	30/03/2022	Second release	C _{ISS} and C _{OSS} values updated
003	18/05/2022	Third release	Part marking

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It is subject to the user's duty of care to design and validate his products in such a way that appropriate measures are taken, such as protective circuits or redundant systems to ensure the safety standards required in the application.

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