

GR-10E003DG: Enhancement Mode Power Transistor

Description

GR-10E003DG is an enhancement mode GaN on Silicon power transistor. 10E003DG provides, high current and high operating speed which is suitable for DC to DC power supply applications.

Key Specifications

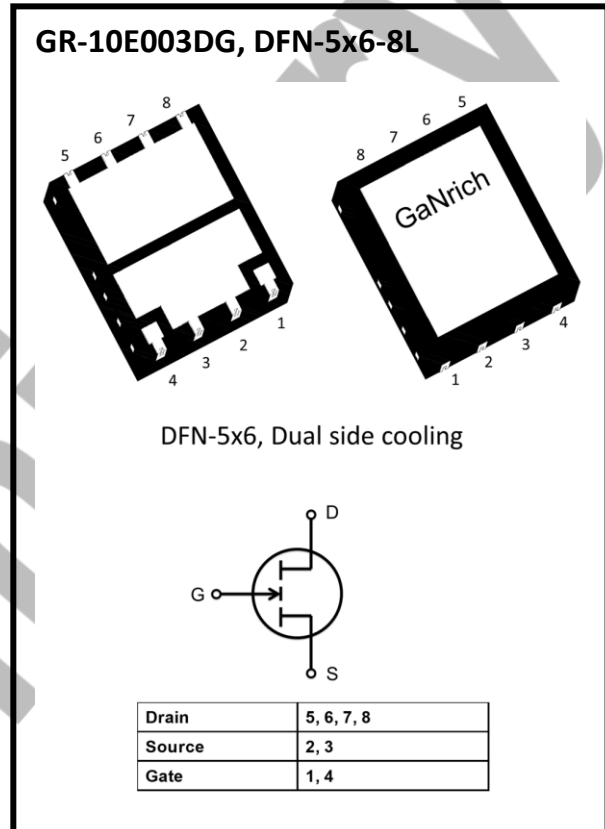
Part Number	GR-10E003DG
V _{DSS} , min.	100V
I _{DS} , Pulse (25°C, TPULSE = 300µs)	150A
R _{DS(ON)} , typ. @VGS=5V	3.1mΩ
Q _G , typ.	13nC

Features

- 100 V enhancement mode power transistor
- High operating frequency
- R_{DS(on)} = Typ. 3.1mΩ
- Dual-side cooled package
- HS compliant

Applications

- Switch Mode Power Supplies (SMPS)
- DC-DC Converters
- Fast Battery Charging
- Appliance Motor Drives



1. Electrical Characteristics

➤ **Table 1 Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-source voltage	100	V
V _{(TR)DSS}	Transient drain to source voltage ^a	120	V
V _{GSS}	Gate- source voltage	-6V ~ +6V	V
I _D	Drain current (continuous) at T _C = 25°C operation	55	A
	Drain current (continuous) at T _C = 100°C operation	38	A
I _{D,Pulse}	Pulsed drain current (pulse width: 300μs, V _{gs} =5V) ^b	150	A
T _J	Operating temperature	-40 to +150	°C
T _S	Storage temperature	-40 to +150	°C
MSL	Moisture sensitivity level	MSL3	

- a. In off-state, spike duty cycle D<0.01, spike duration <1μs
- b. Defined by product design and characterization. Value is not tested to full current in production

➤ **Table 2 Thermal Characteristics**

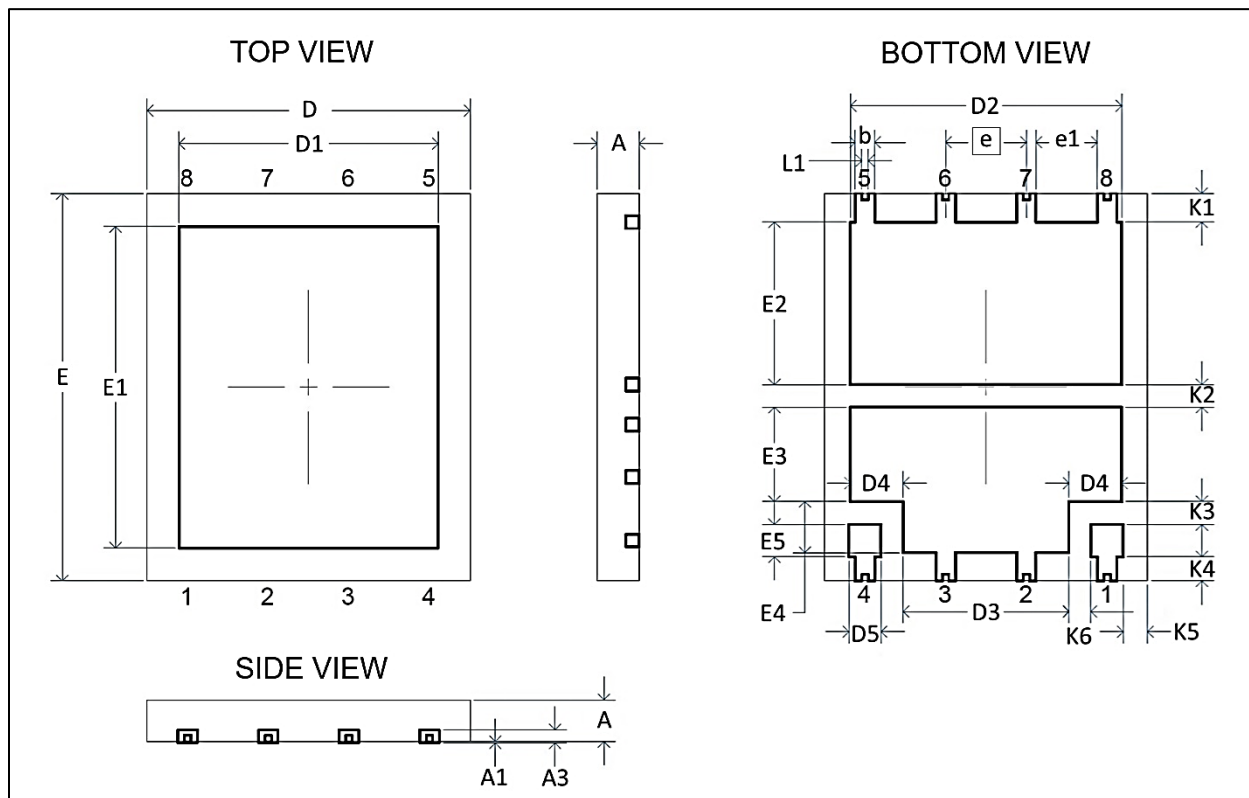
Symbol	Parameter	Value	Unit
R _{θJC (top)}	Thermal resistance junction-case ^a , top	0.30	°C/W
R _{θJC (bottom)}	Thermal resistance junction-case ^a , bottom	0.45	°C/W
R _{θJA}	Thermal resistance junction-ambient ^b	60	°C/W

- a. Tested in package DFN-5x6.
- b. Device on 1 layer PCB.

➤ **Table 3 Electrical Characteristics** ($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise stated)

Symbol	Parameter	Conditions	Values			Unit
			min.	typ.	max.	
BV_{DSS}	Drain-source voltage	$V_{GS} = 0V, I_D = 150\mu A$	100	-	-	V
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 15mA$	0.8	1.1	1.6	V
$R_{DS(on)}$	Drain-source on-resistance	$V_{GS} = 5V, I_D = 50A$	-	3.1	4.0	$m\Omega$
I_{DSS}	Drain-source leakage current	$V_{DS} = 80V, V_{GS} = 0V$	-	5.0	400	μA
I_{GSS}	Gate-to-Source Forward Leakage current	$V_{GS} = +5V$	-	0.080	16.0	mA
	Gate-to-Source Forward Leakage current	$V_{GS} = +5V, T_J = 125^{\circ}\text{C}$	-	0.75	22.5	mA
	Gate-to-Source Reverse Leakage current	$V_{GS} = -4V$	-	0.060	1.8	mA
C_{ISS}	Input capacitance	$V_{DS} = 50V, V_{GS} = 0V$	-	1950	-	pF
C_{OSS}	Output capacitance		-	650	-	
C_{RSS}	Reverse transfer capacitance		-	9.8	-	
Q_G	Gate charge	$V_{DS} = 50V, V_{GS} = 5V, I_D = 50A$	-	13	-	nC
Q_{GS}	Gate-source charge	$V_{DS} = 50V, I_D = 50A$	-	4.5	-	
Q_{GD}	Gate-drain charge		-	1.0	-	
Q_{OSS}	Output charge	$V_{DS} = 50V, V_{GS} = 0V$	-	50	-	
Q_{RR}	Source-Drain Recovery Charge	-	-	0	-	

2. Package Outline Dimensions (DFN-5x6-8L)

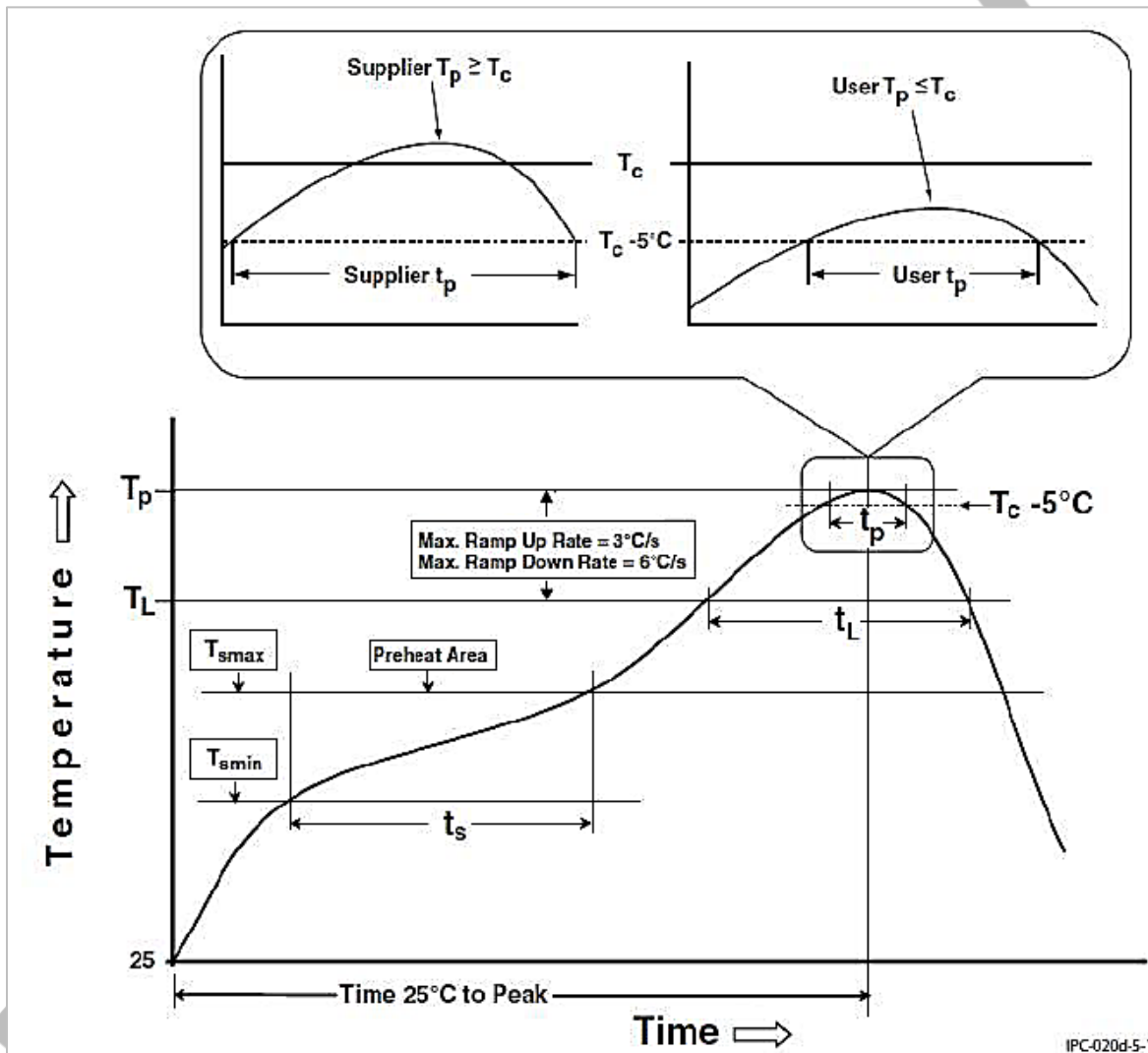


➤ **Table 4 Dimension of GR-DFN-5x6-8L**

SYMBOL	DIMENSION (MM)			SYMBOL	DIMENSION (IN MM)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.60	0.65	0.70	E1	4.977 REF		
A1	--	0.02	0.05	E2	2.42	2.52	2.62
A3	0.203 REF			E3	1.36	1.46	1.56
D	4.90	5.00	5.10	E4	0.69	0.79	0.89
E	5.90	6.00	6.10	E5	0.40	0.50	0.60
e	1.25 BSC			K1	0.34	0.44	0.54
e1	0.85	0.95	1.05	K2	0.25	0.35	0.45
b	0.20	0.30	0.40	K3	0.257	0.357	0.457
D1	4.018 REF			K4	0.273	0.373	0.473
D2	4.10	4.20	4.30	K5	0.275	0.375	0.475
D3	2.468	2.568	2.668	K6	0.241	0.341	0.441
D4	0.716	0.816	0.916	L1	0.05	0.10	0.20
D5	0.40	0.50	0.60	-	-	-	-

3. Reflow Soldering Profile

Recommended Reflow Soldering Condition (IPC/JEDEC J-STD-020D.1)



*According to IPC (IPC-A-610), solder voids are considered to be a defect when the overall calculated area of all voids in any given solder ball/joint is greater than 25% of the total solder ball area.

➤ **Table 5 Recommended Reflow Soldering Condition**

Profile Feature	Pb-Free Assembly
Preheat/Soak	
Temperature Min (T_{smin})	150°C
Temperature Max (T_{smax})	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max.
Liquidous temperature (T_L)	217°C
Time (t_L) maintained above T_L	60-150 seconds
Time (t_p)* within 5°C of the specified classification temperature (T_c)**, see Reflow Soldering Profile above.	30* seconds
Ramp-down rate (T_p to T_L)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

(t_p)* The highest temperature that an individual package body reaches during MSL classification.

(T_c)** The maximum body temperature at which the component manufacturer guarantees the component MSL as noted on the caution and/or bar code label (per J-STD-033).

30* seconds Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in **Table 5**.

For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds

4. Change Log

Version	Date	Description
0.1	March 28, 2025	Initial version
0.2	April 16, 2026	Electrical characteristics revised

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